IP LICENSE AUTHENTICATION, SECURITY CHIP

Manual

Rev	Date	Author	Comments
1.0	7.3.2013	Flexibilis Oy / Jouni Kujala	Initial version
1.1	8.3.2013	Flexibilis Oy / Jouni Kujala	Added the ordering code for the security chip and pointers to Altera documents
1.2	10.6.2013	Flexibilis Oy / Jouni Kujala	F100 package added

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1 About This Document

This document describes the Security Chip method used for the IP License Authentication. The idea is that there is a separate Security Chip connected to the FPGA chip. The IP core at the FPGA sends challenges to the Security Chip, and by evaluating the replies it is able to determine whether the user has a valid license to use the IP core or not.

2 General

To prevent unauthorized use of certain Flexibilis IP blocks, the IP block includes an Authentication Interface. An external Security Chip is connected to the Interface. The IP block sends authentication requests approximately once a second to the connected Security Chip and examines the replies it gets. Valid replies from the Security Chip indicate to the IP block that the user has a valid license to use the IP.

Without a valid license the IP core still works for a certain period, making it possible for customers to evaluate the IP core. The Security Chip method is used with the Flexibilis IP products listed in Table 1.

Flexibilis IP Core	Altera Part Number for Security Chip
FRS (Flexibilis Redundant Switch) [1]	M570ZM6NJA (M100 package)
FRS (Flexibilis Redundant Switch) [1]	M570F11NAA (F100 package)

Table 1. Flexibilis IP Core(s) and Respective Security Chips

Security Chips can be purchased from Altera and from authorized Altera distributors. See contact information at http://www.altera.com/corporate/contact/con-index.html.

2.1 Security Chip Signals

2.1.1 M100 Package

The pinout of the Security chip M570ZM6NJA is presented in Table 2 and in Table 3. The Authentication Interface signals are presented in Table 2.

Signal Name	Direction	Voltage Level	Pin
clk_shift	Input	3.3V LVTTL	E1
chal_valid	Input	3.3V LVTTL	E11
chal_data	Input	3.3V LVTTL	C11
resp_valid	Output	3.3V LVTTL	J11
resp_data	Output	3.3V LVTTL	C1

Table 2. Authentication Interface Signals of Security Chip (EPM570Z in the M100 package)

Connect the Authentication interface signals of Security Chip to Authentication Interface signals of the IP core. The frequency of these signals is approximately 1kHz.

The other pins of the Security Chip are presented in Table 3.

Name	Direction	Usage	Pin
VCCIO	Input	I/O voltage supply. Tie to 3.3V.	E3, J4, J8, G9, C8, C4
VCCINT	Input	CPLD core voltage supply. Tie to 1.8V.	G3, J7, E9, C7
GND	Input	Tie to ground plane.	E4, G4, H5, J5, H7, G8, E8, D7, C5, D5
rst_system_n	Input	Active low reset signal. If not used, tie high. Voltage level 3.3V LVTTL.	G11

Table 3. The other Signals of Security Chip (EPM570Z in the M100 package)

An example on how to connect Security Chip to FPGA and to FRS is presented in Figure 1. Note that the pinout of the FPGA is not fixed; the user can connect the Authentication Interface signals of FRS to any I/O pins of the FPGA.

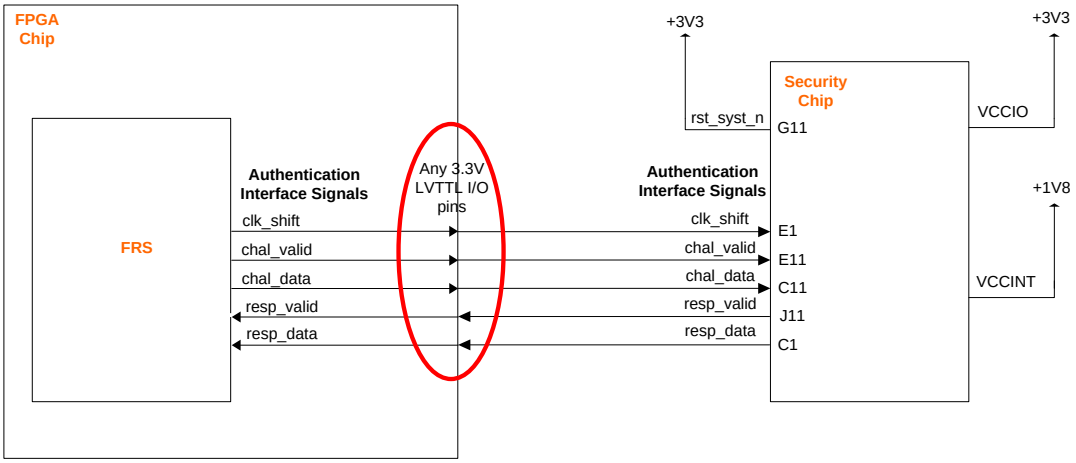

Figure 1. Connecting Security Chip (M100 package) to FRS

The Security Chip M570ZM6NJA is Altera EPM570Z (in the M100 package) factory pre-programmed to function as a Security Chip. See more information on EPM570Z pinout in Altera pin information document [2]. For layout design the M100 package dimensions can be found in Altera Device Package Information document for 100-Pin MBGA [3]. The unused I/O pins of the Security Chip can be either left floating or connected to the ground plane.

2.1.2 F100 Package

The pinout of the Security chip M570F11NAA is presented in Table 4 and in Table 5. The Authentication Interface signals are presented in Table 4.

Signal Name	Direction	Voltage Level	Pin
clk_shift	Input	3.3V LVTTL	E1
chal_valid	Input	3.3V LVTTL	C10
chal_data	Input	3.3V LVTTL	A10
resp_valid	Output	3.3V LVTTL	G10
resp_data	Output	3.3V LVTTL	C1

Table 4. Authentication Interface Signals of Security Chip (EPM570 in the F100 package)

Connect the Authentication interface signals of Security Chip to Authentication Interface signals of the IP core. The frequency of these signals is approximately 1kHz.

The other pins of the Security Chip are presented in Table 5.

Name	Direction	Usage	Pin
VCCIO	Input	I/O voltage supply. Tie to 3.3V.	E4, G4, G6, F7, D6, D4
VCCINT	Input	CPLD core voltage supply. Tie to 3.3V or to 2.5V.	F4, H6, E7, C6
GND	Input	Tie to ground plane.	F5, H5, E6, C5, E5, G5, G7, F6, D7, D5
rst_system_n	Input	Active low reset signal. If not used, tie high. Voltage level 3.3V LVTTL.	E10

Table 5. The other Signals of Security Chip (EPM570 in the F100 package)

An example on how to connect Security Chip to FPGA and to FRS is presented in Figure 2.

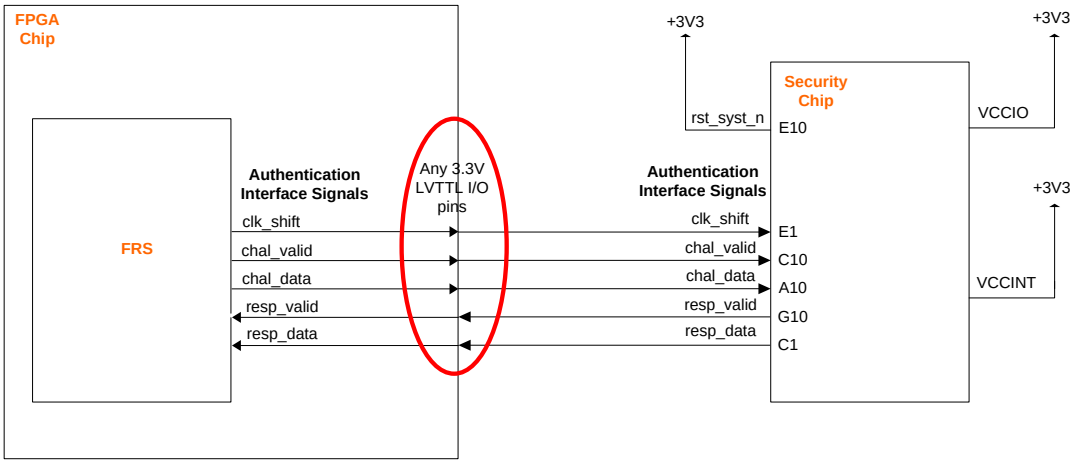

Figure 2. Connecting Security Chip (F100 package) to FRS

The Security Chip M570F11NAA is Altera EPM570 (in the F100 package) factory pre-programmed to function as a Security Chip. See more information on EPM570 pinout in Altera pin information document [4]. For layout design the F100 package dimensions can be found in Altera Device Package Information document for 100-Pin FBGA [5]. The unused I/O pins of the Security Chip can be either left floating or connected to the ground plane.

3 Glossary

CPLD	Complex Programmable Logic Device
FBGA	FineLine Ball-Grid Array
FPGA	Field Programmable Gate Array
FRS	Flexibilis Redundant Switch
I/O	Input/Output
IP	Intellectual Property
LVTTL	Low Voltage Transistor-Transistor Logic
MBGA	Micro FineLine Ball-Grid Array

4 References

[1] "FRS Manual", Flexibilis Oy, 2013

[2] "Altera MAX IIZ EPM570Z Pin information", Altera Corporation, version 1.0, http://www.altera.com/literature/dp/max2/EPM570Z.pdf

[3] "Altera Device Package Information" describing 100-Pin MBGA, Altera Corporation, version 1.0, July 2011, http://www.altera.com/devicepackaging/04R00345-01.pdf

[4] "Altera MAX II EPM570 / EPM570G Pin information", Altera Corporation, version 1.4, http://www.altera.com/literature/dp/max2/EPM570.pdf

[5] "Altera Device Package Information" describing 100-Pin FBGA, Altera Corporation, version 2.0, November 2011, http://www.altera.com/devicepackaging/04R00223-02.pdf