Advanced Flexibilis Ethernet Controller (AFEC)

Release Note

Contents

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1 About This Document

This document contains Advanced Flexibilis Ethernet Controller (AFEC) release information. Chapter 2 contains release information, release content and instructions how to use release. Chapter 3 contains release history.

2 General

2.1 Release Information

IP Name	AFEC
Release	1.4
Date	10.9.2015

Table 1. Release information

2.2 Release Content

Module/Document/Part	Version	REV ID
afec.vhd	1.4	AFEC Revision ID: 0x07* (register GENERAL) AFEC Configuration ID number : 1* (register CFG_ID) AFEC Configuration rev: 3838* (register CFG_ID) AFEC Body rev: 3837* (register SUB_ID)
AFEC_user_manual.pdf	1.2	AFEC User Manual

Table 2. Release content

* Readable from IP core

2.3 Installation and Configuration

2.3.1 Module Instantiation

The top level entity with the default generics:

```
entity afec is
  generic(
    -- Polarity
    RST_ACTIVE : integer := 1;
    DESC_MSB : integer   := 2;
    -- Resource usage
    FIFO_ADDR_MSB : integer := 10;
    DEVICE_FAMILY : string  := "";
    MEM_INIT_FILE : string  := ""
    );
  port(
    -- Main
    rst : in std_logic; -- system reset
    clk : in std_logic; -- system clock
    -- Clock mux control
    gtx_clk_sel : out std_logic; -- transmit clock select
    -- GMII/MII
    rx_rst : in  std_logic;                    -- receive reset
    rx_clk : in  std_logic;                    -- receive clock
    rx_dv  : in  std_logic;                    -- receive data valid
    rxd    : in  std_logic_vector(7 downto 0); -- receive data
    rx_er  : in  std_logic;                    -- receive error
    tx_rst : in  std_logic;                    -- transmit reset
    tx_clk : in  std_logic;                    -- transmit clock
    tx_en  : out std_logic;                    -- transmit enable
    txd    : out std_logic_vector(7 downto 0); -- transmit data
    tx_er  : out std_logic;                    -- transmit error
    crs    : in  std_logic;                    -- carrier
    col    : in  std_logic;                    -- collision
    -- Symbol alignment
    tx_alignment : in std_logic;
    -- Time
    rx_time_req  : out std_logic;
    rx_time_ack  : in  std_logic;
    rx_time_word : in  std_logic_vector(95 downto 0);
    tx_time_req  : out std_logic;
    tx_time_ack  : in  std_logic;
    tx_time_word : in  std_logic_vector(95 downto 0);
    -- MII Management
    mdio_in  : in  std_logic; -- management data input
    mdio_out : out std_logic; -- management data output
    mdio_ena : out std_logic; -- management data output enable
    mdc      : out std_logic; -- MDIO clock, max freq 2,5 MHz
    -- Bus, Avalon master port, tx DMA
    tx_m_address      : out std_logic_vector(31 downto 0);
    tx_m_byteenable   : out std_logic_vector(7 downto 0);
    tx_m_read         : out std_logic;
    tx_m_readdata     : in  std_logic_vector(63 downto 0);
    tx_m_waitrequest  : in  std_logic;
    -- Bus, Avalon master port, rx DMA
    rx_m_address     : out std_logic_vector(31 downto 0);
    rx_m_byteenable  : out std_logic_vector(7 downto 0);
    rx_m_write       : out std_logic;
    rx_m_writedata   : out std_logic_vector(63 downto 0);
    rx_m_waitrequest : in  std_logic;
    -- Bus, Avalon slave port, MMUR
    s_cs          : in  std_logic;
    s_address     : in  std_logic_vector(13 downto 0);
    s_byteenable  : in  std_logic_vector(7 downto 0);
    s_read        : in  std_logic;
    s_readdata    : out std_logic_vector(63 downto 0);
    s_write       : in  std_logic;
    s_writedata   : in  std_logic_vector(63 downto 0);
    s_waitrequest : out std_logic;
    -- Interrupt
    irq : out std_logic
    );
end afec;
```

3 Release History

Date	Revision	Description and changes
10.9.2015	1.4	- Number of descriptors set configurable, available values 8 and 16
19.12.2014	1.3.1	- Opencore plus license updated
9.12.2013	1.3	- Opencore plus license updated
9.8.2013	1.2	- Minor internal updates
15.5.2013	1.1	- Product naming update - Minor internal updates
8.8.2011	1.07	- Added support for 16-bit Avalon-MMUR commands (the interface data width remains fixed 64-bit)
12.1.2011	1.06	- Added support for GMII-RGMII adapter
21.12.2010	1.05	- Added support for MII-RMII adapter
25.3.2010	1.04	- BUG FIX: Tx data overwrite fixed for back-to-back packets (caused overwrite failures when high traffic)
22.3.2010	1.03	- BUG FIX: SFD synchronization fixed for 10/100 Mbps
8.10.2009	1.02	- Early Rx DMA now enabled - Rx Descriptor error in chain 1 causes now frame termination with Size Error flag up instead of Descriptor Error interrupt - External EIF error added to Rx descriptor - Minor Cleanup
4.9.2009	1.01	- Rx post processing re-designed to cope with slow Rx DMA - Internal option added to disable early DMA, currently disabled - Default generic for FIFO_SIZE increased to 2048 bytes
10.8.2009	1.00	Initial Release

Table 3. Release history