

# **FLEXIBILIS ETHERNET SWITCH (FES)**

## **Altera Cyclone IV Demo**

This document could contain technical inaccuracies or typographical errors. Flexibilis Oy may make changes in the product described in this document at any time.

Please, email comments about this document to [support@flexibilis.com](mailto:support@flexibilis.com).

© Copyright Flexibilis Oy 2013. All rights reserved.

#### **Trademarks**

All trademarks are the property of their respective owners.

## Contents

---

<b>1 Introduction .....</b>	<b>6</b>
<b>2 Equipment Needed .....</b>	<b>7</b>
<b>3 Software Needed.....</b>	<b>9</b>
<b>4 Setting up the Evaluation .....</b>	<b>10</b>
4.1 DIP Switches.....	10
4.2 Connecting the Boards and Cables .....	12
4.3 Configuring the FPGA Board .....	14
4.4 Configuring IP Addresses .....	14
<b>5 Testing .....</b>	<b>16</b>
5.1 Testing the Connection .....	16
5.2 LCD Display .....	16
5.2.1 First View.....	17
5.2.2 Second View .....	17
5.2.3 Third View.....	17
5.2.4 Fourth View .....	17
5.2.5 Fifth View.....	17
5.2.6 Sixth View.....	18
<b>6 Troubleshooting .....</b>	<b>19</b>
6.1 Programming Hardware Cable Not Detected .....	19
6.2 Program Does not Load.....	19
6.3 Link Does not Go up .....	19
6.4 File Transfer/Ping Does not Work.....	20
<b>7 Known Issues.....</b>	<b>22</b>
<b>8 Appendix 1 External MDIO.....</b>	<b>23</b>
<b>9 Appendix 2 Reference Design .....</b>	<b>24</b>
9.1 Installing .....	24
9.2 Using with Quartus.....	24
9.3 Block Diagram.....	24
9.4 Main Blocks.....	25
9.4.1 FES.....	26
9.4.2 AFEC .....	26
9.4.3 FRTC .....	26
9.4.4 NIOS2 (xr7_softsoc) .....	26
9.4.5 gmii_to_rgmii .....	26
9.4.6 gmii_to_alt_tse .....	26
9.5 How to Modify the Design .....	26
9.6 How to Compile the Design and Download to the Board .....	27
9.7 The Licenses Needed and How to Get them.....	27

## Figures

---

Figure 1. SFP Module for Multimode Fiber Optic Cable (Black Latch) .....	7
Figure 2. SFP Module for Single Mode Fiber Optic Cable (Blue Latch).....	7
Figure 3. SFP Module for Copper Cable .....	7
Figure 4. Altera Quartus II Software .....	9
Figure 5. FES Evaluation Setup .....	10
Figure 6. DIP Switch 1 and 2 Settings.....	11
Figure 7. SFP HSMC Board DIP Settings .....	12
Figure 8. Connecting the Boards.....	13
Figure 9. Port Numbering of SFP HSMC Board .....	13
Figure 10. PGM_SEL and PGM_LOAD Buttons .....	14

Figure 11. Checking IPv4 Address .....	15
Figure 12. Ping Is Working .....	16
Figure 13. PB0 –button to change the screen view.....	16
Figure 14. Red Circle Indicates the Link LEDs.....	19
Figure 15. Crossover Cable.....	20
Figure 16. Straight Cable.....	20
Figure 17. Two Laptops Connected .....	21
Figure 18. HSMC Debug Header Breakout Board .....	23
Figure 19. Reference Design Block Diagram .....	25

## ***Tables***

---

Table 1. Usage of the SW2 DIP Switches .....	12
Table 2. Pinout of the connector (MDIO).....	23

## ***Revision History***

---

Rev	Date	Comments
1.0	18.04.2013	First version
1.1	10.10.2013	Updates due to updates in the reference design

## 1 Introduction

This document contains instructions on an evaluation setup that can be used for evaluating functionality of Flexibilis Ethernet Switch (FES), an FPGA IP core from Flexibilis Oy (Inc.). This document is targeted for anyone who wishes to build such a test setup.

Flexibilis Ethernet Switch (FES) is a triple-speed (10Mbps/100Mbps/1Gbps) Ethernet Layer 2 switch IP with gigabit forwarding capacity per port. FES is compatible with IEEE 1588v2 end-to-end and peer-to-peer transparent clock functionality, which significantly improves the ability to fight degradation of clock information quality in large networks. FES is available in several different configurations, from 3-port to 8-port. For more information, please see the manual: [http://www.flexibilis.com/downloads/FES\\_manual.pdf](http://www.flexibilis.com/downloads/FES_manual.pdf).

For evaluation purposes FES is available as a 4-port configuration ready compiled for Altera Cyclone IV GX FPGA Development Kit. If you want to test with a different configuration, please contact us. With these instructions, a simple network between (up to) four Ethernet devices and one FPGA board can be constructed.

## 2 Equipment Needed

The following is the minimum equipment needed for building the evaluation setup (see the next page for information on where they can be ordered from).

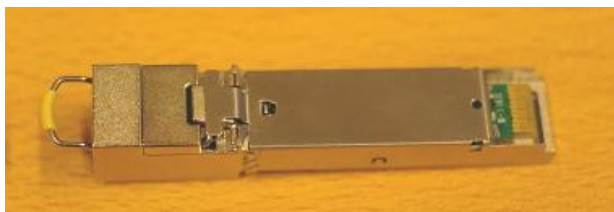
- One Cyclone IV GX FPGA Development Kit
- One Terasic SFP HSMC Board
- Power adapter for the FPGA board (comes with the Development Kit)
- USB cable for programming the board (comes with the Development Kit)
- Four Ethernet devices (For example laptop, web camera or test equipment that is able to send/receive Ethernet frames)
- Four Ethernet cables. One has to be copper cable, the rest can be fiber or copper, single or multimode, depending on the devices used. If you are using e.g. laptops, you need copper cables.
  - All copper cables should be crossover type.
- 3 SFP modules. They can be fiber (see Figure 1 and Figure 2) or copper SFP modules (see Figure 3) depending on what kind of cables are used (fiber or copper).
- A computer with USB connector for programming the evaluation board (this can be one of the above mentioned Ethernet devices)
- Three 8mm standoffs and four 15 mm standoffs (little metal feet the board can stand on) and seven metal nuts (0.217"/5.51mm, M3) for the standoffs.



**Figure 1. SFP Module for Multimode Fiber Optic Cable (Black Latch)**



**Figure 2. SFP Module for Single Mode Fiber Optic Cable (Blue Latch)**



**Figure 3. SFP Module for Copper Cable**

Note that touching or moving the boards during operation may cause frame loss. This is because of disturbance to the board-to-board signals.

The following lists the recommended places where from the equipment needed can be ordered from:

- Cyclone IV GX FPGA Development Kit from Altera (ordering code DK-DEV-4CGX150N): <http://www.altera.com/products/devkits/altera/kit-cyclone-iv-gx.html>

- USB cable and power adapter for the board is included in the Cyclone IV GX FPGA Development Kit.
- Terasic SFP HSMC Board: <http://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&CategoryNo=71&No=342>
- SFP module for multimode fiber cable from Digi-Key: <http://www.digikey.com/product-search/en?x=15&y=12&lang=en&site=us&Keywords=afbr-5715alz>. Typically multimode cables are orange in color and the SFP module latch is black (see Figure 1).
- SFP module for single mode fiber cable from Digi-Key: <http://www.digikey.com/product-search/en?x=15&y=12&lang=en&site=us&Keywords=afct-5715alz>. Typically single mode cable is yellow in color and the SFP module latch is blue (see Figure 2).
- SFP module for copper cable from Digi-Key: <http://www.digikey.com/product-search/en?x=28&y=20&lang=en&site=us&Keywords=FCLF-8521-3>
- Single mode fiber optic cable from Digi-Key: <http://www.digikey.com/product-detail/en/1435791-1/1435791-1-ND/1889887>
- Multimode fiber optic cable from Digi-Key: <http://www.digikey.com/product-detail/en/9-6374659-7/9-6374659-7-ND/2326175>
- Copper crossover cable (RJ45) from Digi-Key: <http://www.digikey.com/product-detail/en/219153-1/219153-1-ND/1892833>
- 8 mm standoff from Digi-Key: <http://www.digikey.com/product-detail/en/R30-3000802/952-1499-ND/2264480>
- 15 mm standoff from Digi-Key: <http://www.digikey.com/product-detail/en/R30-3001502/952-1506-ND/2264487>
- 0.217" (5.51mm) M3 nuts from Digi-Key: <http://www.digikey.com/product-detail/en/MHNZ%20003/H762-ND/274973>

The whole packet including everything necessary for the evaluation can also be ordered from Flexibilis. Please contact [contact@flexibilis.com](mailto:contact@flexibilis.com) for further information.

For the Terasic boards you can also contact local Altera distributors.

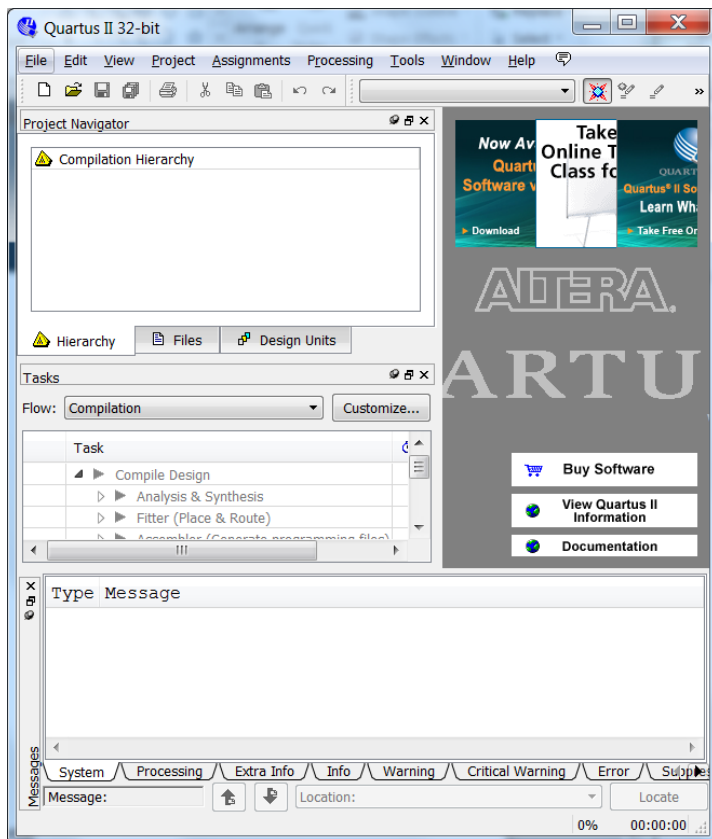


### 3 Software Needed

All the software mentioned here should be located on the computer that will be used for programming the boards. It can be one of the test devices or a separate computer not connected to the network.

The programming file is included in the Reference Design packet that can be downloaded from this link: <http://www.flexibilis.com/downloads/refdesigncheck.php>. Save the file somewhere on the computer; the location of the file doesn't matter.

Next you should download and install Altera Quartus II software if you do not have it installed already. Free web edition can be downloaded at [www.altera.com/support/software/download/sof-download\\_center.html](http://www.altera.com/support/software/download/sof-download_center.html). Figure 4 shows what the user interface of the software looks like.



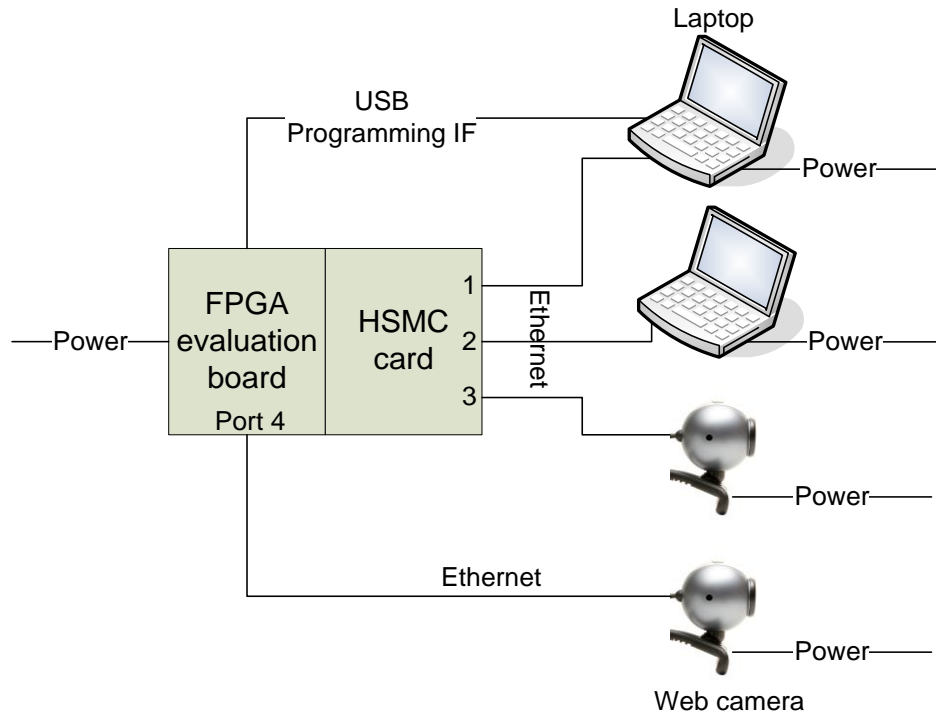
**Figure 4. Altera Quartus II Software**

Administrator rights are needed to be able to install the software. Please note that installing the software might take a few hours and Internet connection is needed for the duration of the installation process.

## 4 Setting up the Evaluation

If you haven't used Altera boards before, the documentation might be useful as it contains some instructions. It can be downloaded at: [www.altera.com/products/devkits/altera/kit-cyclone-iv-gx.html](http://www.altera.com/products/devkits/altera/kit-cyclone-iv-gx.html).

See Figure 5 for an example of the whole setup.



**Figure 5. FES Evaluation Setup**

First you should connect the HSMC board to the FPGA board (use HSMC A connector). Using standoffs with the boards is recommended but not absolutely necessary. The 15 mm standoffs should go under the HSMC board and the 8 mm standoffs under the FPGA board. Use the nuts to tighten the standoffs to the boards.

If you want to access FES registers (not necessary for the evaluation), you can do this by connecting the MDIO. The MDIO can be connected with the HSMC Debug Header Breakout Board that comes with the Altera Development Kit (use HSMC B connector as in Figure 18). See Table 2 at the end of the document for the pinout of the connector. Also see [www.terasic.com.tw/cgi-bin/page/archive\\_download.pl?Language=China&No=495&FID=6266b5c8147aac2f821702f97c440dc8](http://www.terasic.com.tw/cgi-bin/page/archive_download.pl?Language=China&No=495&FID=6266b5c8147aac2f821702f97c440dc8) for the schematics of the board. The DIP switch SW2.5 is used to select where to the MDIO is connected, see Table 1.

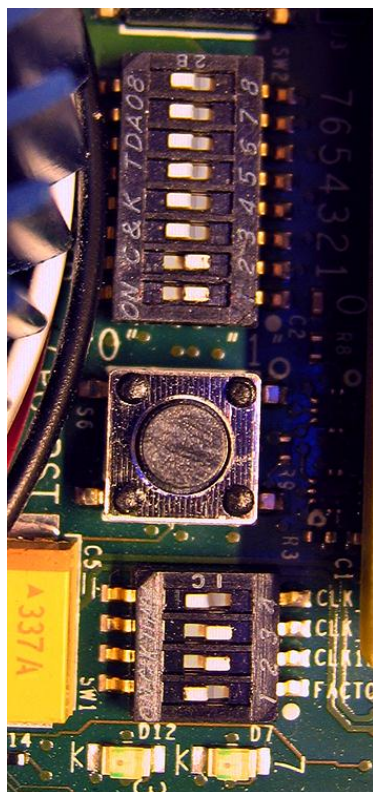
### 4.1 DIP Switches

Check the DIP switches on the FPGA board.

DIP setting for SW1 and SW2 (see Figure 6):

- SW1.1 USER\_FACTORY "ON" ("0")
- SW1.2 CLK125\_EN "OFF" ("1")
- SW1.3 CLKA\_EN "OFF" ("1")
- SW1.4 CLK\_SEL "ON" ("0")
- SW2.1 "OFF" ("1")
- SW2.2 "OFF" ("1")

- SW2.3 – SW2.8 “ON” (“0”)



**Figure 6. DIP Switch 1 and 2 Settings**

SW4 and SW5 can be left at their default settings. SW3 is the power switch (on/off). For more information on the DIP switches you can check the documentation of the development board (<http://www.altera.com/products/devkits/altera/kit-cyclone-iv-gx.html>). Also see Table 1 that presents the usage of SW2 switches.

Switch (as presented in Altera documentation)	Usage	Printed on the DIP switch component	Printed on the circuit board
SW2.1	Selects the mode for redundant ports (port 1 and port 2)  ON: Redundant ports are in PRP mode  OFF: Redundant ports are in HSR mode  This selection is valid only when SW2.2 is ON.	1	0
SW2.2	ON: Flexibilis Redundant Switch (FRS), ports 1 and 2 are in PRP or HSR mode, depending on SW2.1  <b>OFF: Flexibilis Ethernet Switch (FES), all ports are normal Ethernet</b>	2	1
SW2.3	ON: port 3 is in PRP interlink mode	3	2

	OFF: port3 is in HSR interlink mode This selection is valid only when both SW2.2 and SW2.4 are ON.		
SW2.4	Selects the mode for port 3 (together with SW2.3). ON: port 3 is in PRP or HSR interlink mode (depending on SW2.3) OFF: port3 is in normal (non-HSR, non-PRP) Interlink mode. This selection is valid only when SW2.2 is ON.	4	3
SW2.5	<b>ON: Normal mode. The internal NIOS processor accesses the registers of FES. Do not use the external MDIO interface.</b> <b>OFF: The internal NIOS processor won't access FES registers. The external MDIO can be used to access the registers.</b>	5	4
SW2.6	This DIP selects the PRP NetId for the attached PRP network. Only valid when configured into PRP interlink mode (SW2.3 and SW2.4). ON: NetId = 1 OFF: NetId = 2	6	5
SW2.7-SW2.8	Reserved for future use.	7-8	6-7

**Table 1. Usage of the SW2 DIP Switches**

The SFP HSMC board DIP switches can be at default position, see Figure 7 for reference.

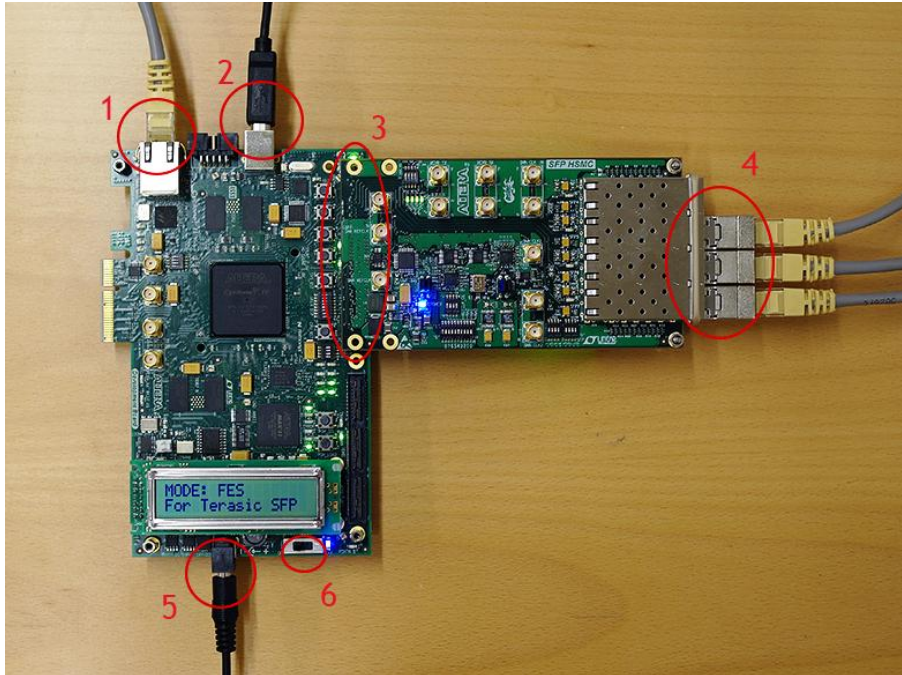


**Figure 7. SFP HSMC Board DIP Settings**

## 4.2 Connecting the Boards and Cables

First you should connect the HSMC board to the FPGA board. Use HSMC A connector as presented in Figure 8. In Figure 8:

1. Ethernet Port 4 (RJ45)
2. USB port/cable
3. HSMC connector A
4. Ethernet Ports 1-3 (SFP)
5. Power cable
6. Power switch (On/Off)

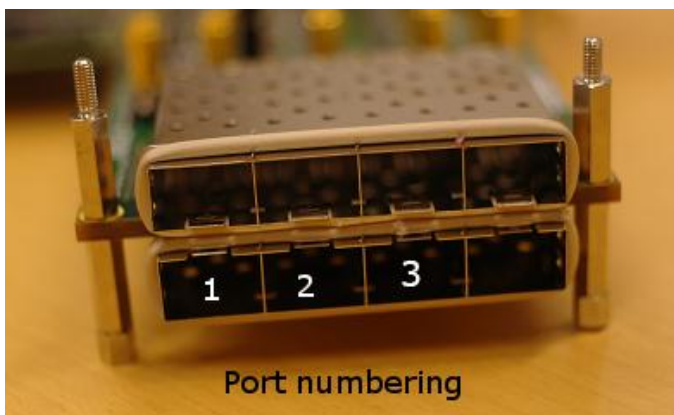


**Figure 8. Connecting the Boards**

Connect the USB cable between the FPGA board and the PC used for programming. It can be a separate computer or one of the Ethernet devices in the network. Next, connect the power cable to the FPGA board.

Attach Ethernet cables from the SFP board ports 1-3 to the Ethernet devices. To be able to attach the cables to the SFP board you need to use the SFP modules. Attach a cable from port 4 (RJ45) to the fourth Ethernet device.

Figure 9 shows the SFP HSMC board port numbering.



**Figure 9. Port Numbering of SFP HSMC Board**



### 4.3 Configuring the FPGA Board

Turn on the FPGA board. Unzip/extract the FESHA00E00-FBIT.zip packet somewhere on the computer used for programming if you haven't done so already. Then open the NIOS command prompt, located at somewhere like **Start -> All Programs -> Altera -> Nios II EDS 13.0 -> Nios II 13.0 Command Shell**.

The packet contains a folder named "cyclone4GXdevkit\_softsoc" and under that there is a folder named "script". You have to change to this "script"-directory in the NIOS command shell. You can move from one directory to another with the command **cd**. To get to Windows root directory you should type **/cygdrive** at the beginning.

For example, if the packet was extracted to C:\users\you\downloads\FESHA00E00-FBIT, type

```
cd /cygdrive/c/users/you/downloads/FESHA00E00-FBIT/cyclone4GXdevkit_softsoc/script
```

Command **pwd** shows in which directory you are in right now. So now if you type **pwd** and press enter, it should show you "/cygdrive/c/users/you/downloads/FESHA00E00-FBIT/cyclone4GXdevkit\_softsoc/script".

Run the flashing script by typing **./flash\_dev\_board.sh TSFP**. This will load the FPGA configuration program to the flash memory of the board.

Wait for the script to finish. This can take for about 10 minutes. After it has finished, you can unplug the USB cable from the FPGA board (not necessary).

After you have run the flashing script, turn the board off. Then turn it on again.

Now the FPGA program should load itself from the Flash memory to the FPGA. If the LCD Screen shows "MODE: FES", the program has been loaded from the Flash memory to the FPGA correctly. If not, you have to load the user configuration from the Flash memory at the board to the FPGA chip using the pushbuttons. You can do this by first pressing PGM\_SEL button. With the button you can go through and select between three alternatives, select "USER" (the LED above text "USER" is on). Then press PGM\_LOAD once to load the user configuration. See Figure 10 or Altera Manual for reference.



Figure 10. PGM\_SEL and PGM\_LOAD Buttons

### 4.4 Configuring IP Addresses

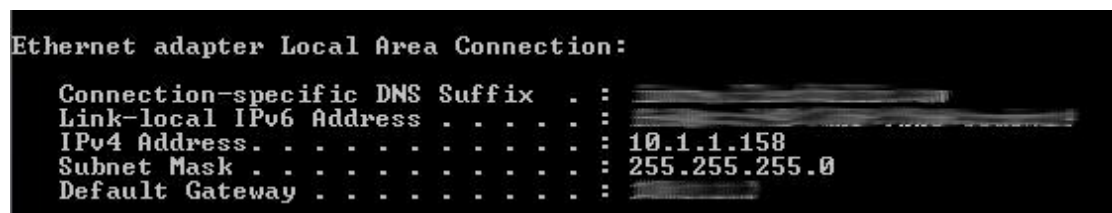
The devices connected to the FPGA board should be in the same IP subnetwork. When the subnet mask is 255.255.255.0 the computers are in the same subnetwork if the first three

parts of the address are the same and only the numbers after the last dot are different. This is the case for example with IP addresses 192.168.0.1 and 192.168.0.2.

A static IP address should be defined for all the devices. For computers with Windows 7, this can be done at **Start -> Control Panel -> Network and Internet -> Network and Sharing Center -> Change adapter settings -> Local Area Connection -> Properties -> Internet Protocol Version 4 -> Use the following IP address**. Administrator rights are needed to be able to change the IP address. If you are using some other device, like a web camera, check from its instruction manual how to change its IP address. Alternatively you can check its default IP address from the manual and change the IP address of the other devices so that they are in the same subnetwork.

You can change the IP addresses for example to 192.168.0.1 (the first device), 192.168.0.2 (the second), 192.168.0.3 (the third), 192.168.0.4 (the fourth device) and the subnet mask to 255.255.255.0 for all the devices.

In Windows 7, the current IP address of the computer can be checked at **Start -> All Programs -> Accessories -> Command prompt**. Type **ipconfig** and press enter. This will show you all the IP addresses of the computer. Search for the line that says "Ethernet adapter Local Area Connection" and under that you can see the IPv4 address and the subnet mask (see Figure 11).



```
Ethernet adapter Local Area Connection:
    Connection-specific DNS Suffix  . : 
    Link-local IPv6 Address . . . . . : 
    IPv4 Address. . . . . : 10.1.1.158
    Subnet Mask . . . . . : 255.255.255.0
    Default Gateway . . . . . :
```

Figure 11. Checking IPv4 Address

## 5 Testing

### 5.1 Testing the Connection

At this point your setup is ready to be tested. This can be done by transferring traffic of some sort, for example by FTP if you have FTP server and client installed. Another possibility is to ping from one computer to another.

In Windows 7, you can ping another computer or another device by first opening the command prompt (**Start -> All Programs -> Accessories -> Command prompt**). Then type **ping** and the IP address you are trying to connect to (for example **ping 192.168.0.2**) and press enter. Figure 12 shows how the response looks like if everything works correctly.

```
C:\Users\>ping 10.1.1.199

Pinging 10.1.1.199 with 32 bytes of data:
Reply from 10.1.1.199: bytes=32 time=1ms TTL=64
Reply from 10.1.1.199: bytes=32 time<1ms TTL=64
Reply from 10.1.1.199: bytes=32 time=1ms TTL=64
Reply from 10.1.1.199: bytes=32 time=1ms TTL=64

Ping statistics for 10.1.1.199:
    Packets: Sent = 4, Received = 4, Lost = 0 (0% loss),
    Approximate round trip times in milli-seconds:
        Minimum = 0ms, Maximum = 1ms, Average = 0ms
```

Figure 12. Ping Is Working

By typing **ping 192.168.0.2 -t** you can ping until **CTRL+C** is pressed.

There is a time limit of **2 hours** for the evaluation. After the time runs out, the board stops working. If this happens, just turn off the board and then turn it on again (then load the user program by using PGM\_SEL and PGM\_LOAD if needed). This will reset the FPGA and it starts counting the evaluation period from the beginning.

After the FPGA program has been programmed to the flash memory of the board once, there is no need to do it again except when upgrading to newer version. The FPGA program needs to be programmed again also if some other program file was programmed to the FPGA board user configuration.

### 5.2 LCD Display

The LCD display of the FPGA board shows the status of the board and the Ethernet interfaces. There are six different views. The view can be changed with the PB0 –button on the FPGA board (see Figure 13). It is the fourth button counted from the PCIe back plate (if installed).

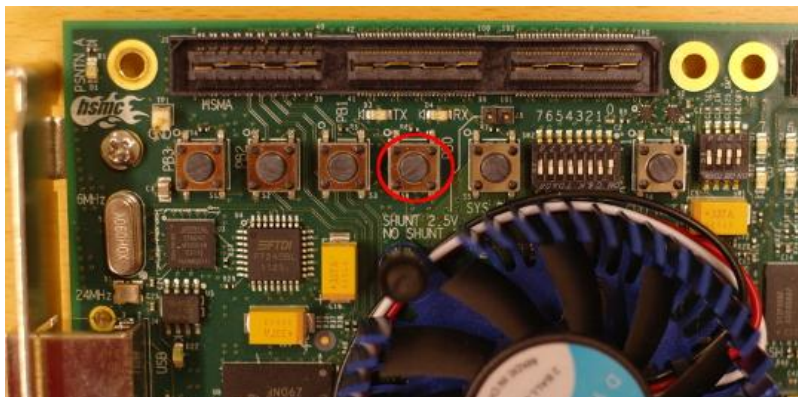


Figure 13. PB0 –button to change the screen view



### 5.2.1 First View

The first view tells the mode the FPGA board. It should look like this:

```
MODE: FES
For Terasic SFP
```

If it shows something else, some of the DIP switches might be in wrong position (see section 4.1).

### 5.2.2 Second View

The second view shows the version number of the IP core and the reference design (REF) currently on the board. It can look for example like this:

```
IP: 2.3.2 17037
REF: 1.1 17048
```

### 5.2.3 Third View

The third view shows the interface speed on each port. P0 means the internal port used by the NIOS softcore CPU. P1 is the SFP port 1, P2 is the SFP port 2 and P3 is the SFP port 3 as indicated in Figure 9. P4 is the Ethernet port (RJ45) on the FPGA board. The view can look for example like this:

```
P0: Autoneg 100
P1: Autoneg 1000
P2: Autoneg 1000
P3: Link down
P4: Autoneg 1000
```

The different options for port mode are “Autoneg 1000”, “Autoneg 100”, “Autoneg 10” and “Link down”.

### 5.2.4 Fourth View

The fourth view can look for example like this:

```
P0 TX 14623
P0 RX 14623
P1 TX 29246
P1 RX 14623
P2 TX 29246
P2 RX 14623
P3 TX 0
P3 RX 0
P4 TX 0
P4 RX 0
```

The numbers after “TX” and “RX” indicate how many packets have been received from and transmitted to each port. P0 means the internal port used by the NIOS softcore CPU. P1 is the SFP port 1, P2 is the SFP port 2 and P3 is the SFP port 3 as indicated in Figure 9. P4 is the Ethernet port (RJ45) on the FPGA board.

### 5.2.5 Fifth View

The fifth view tells how many frames with errors in them have been received and transmitted. OW means an overflow: it indicates that there has been too much traffic compared to the capacity of the link.

```
P0 TXE 0 RXE 0
P0 OW 0
```

P1 TXE 0 RXE 0  
P1 OW 0  
P2 TXE 0 RXE 0  
P2 OW 0  
P3 TXE 0 RXE 0  
P3 OW 0  
P4 TXE 0 RXE 0  
P4 OW 0

P0 means the internal port used by the NIOS softcore CPU. P1 is the SFP port 1, P2 is the SFP port 2 and P3 is the SFP port 3 as indicated in Figure 9. P4 is the Ethernet port (RJ45) on the FPGA board.

### 5.2.6 Sixth View

The sixth view tells the PTP synchronization status. OffM means the offset from the master clock in nanoseconds and P0, P1, P2 and P3 indicate the measured P2P mode peer delay in nanoseconds.

OffM: 15

P0: 319

P1: 312

P2: 0

P3: 0

## 6 Troubleshooting

### 6.1 Programming Hardware Cable Not Detected

- Check the USB cable between the programmer PC and the Altera evaluation board
- Check the POWER LED on the Altera board
- Check the USB\_DISABLE switch on the board (USB should not be disabled)
- Change the programming cable number in the file named "environ" (can be found from the FESHA00E00-FBIT packet, script –folder. The file can be opened with a text editor), line 20, try:
  - CABLE="--cable=0"
  - CABLE="--cable=1"
  - CABLE="--cable=2"

### 6.2 Program Does not Load

- Check that all the DIP Switches are in the right position.
- Try using the PGM\_SEL and PGM\_CONFIG buttons to select and load the user program.
- Try running the flashing script again, and make sure that the board is on and connected to the programming computer with an USB cable while you do so.

### 6.3 Link Does not Go up



**Figure 14. Red Circle Indicates the Link LEDs**

Figure 14 shows the LEDs that indicate if a link is up or not (in other words, if the cable is connected). The LEDs and the corresponding links are:

- D4: HSMCA\_RX: Port 1 (see Figure 9)
- D3: HSMCA\_TX: Port 2 (see Figure 9)
- D6: HSMCB\_RX: Port 3 (see Figure 9)
- D5: HSMCB\_TX: Port 4 (RJ45 port at the FPGA board)

Note that in case copper SFP modules are used, the link LED indicates the status of the link between the FPGA and the (PHY chip inside the) SFP module, while the LCD display shows the status of the link between the SFP module and the other end. So, if a copper SFP module is connected to the board, but there is no cable connected to the module, the link LED will be on and the LCD display shows link down.

The LCD display is presented in section 5.2.

Also computers typically have link LEDs. They are usually located next to the Ethernet port and they should be on when the link is up.

If a link LED is not on even though it should be:

- Check that all the cables and SFP modules are properly attached and the board is switched on
- Check that fiber modules and cables are of the same type
  - Single mode fiber is typically yellow and it should be used only with single mode modules who typically have blue latches, see Figure 2
  - Multimode fiber is typically orange in color and it should be used only with multimode modules who typically have black latches, see Figure 1
- Try changing the cables
- The copper cable has to be crossover type, so check the cable type. Crossover cable (see Figure 15) has different pinouts at each end, which means that the colored lines (wires) you can see through the plastic at the end of the cable (green, blue, red) are in different order at different ends of the cable. On the other hand, straight cables have the same pinout on both ends. You can see this in Figure 16: on both ends the colored lines at the end of the cable are in order green – blue – red.



Figure 15. Crossover Cable

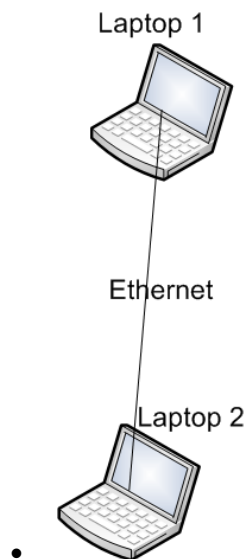


Figure 16. Straight Cable

## 6.4 File Transfer/Ping Does not Work

- Check that all the links are up
- Check the IP addresses: are the computers in the same subnetwork or is there something else wrong with the addresses? See section 4.4 Configuring IP Addresses for how to define the IP addresses.
- Check that file transfer/ping works with straight connection between computers/other devices (connect the two computer/devices to each other with a crossover copper cable, see Figure 17)
- Check the firewall settings of the computers. Try disabling the firewall and see if file transfer/ping starts working.

- There is a time limit of 2 hours for the evaluation. If this time runs out the network will stop working. To get it to working again, turn off the board and then turn it on again and load the user program.



**Figure 17. Two Laptops Connected**

## 7 Known Issues

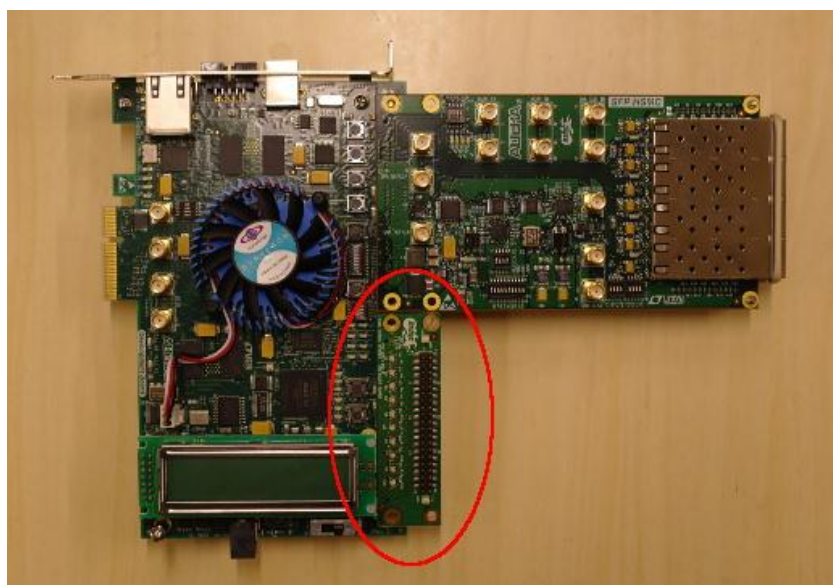
Automatic loading of the user configuration might not be working if the FPGA board has an old version of the CPLD code. Follow Altera instructions on how to update the CPLD configuration if automatic loading of the user configuration at startup is needed.

## 8 Appendix 1 External MDIO

Signal	HSMC Debug Header Breakout Board	HSMC-connector (B)	FPGA
mmd_mdc = Management Data Clock	Header J1, Pin 3	Pin 43	Pin AD29
mmd_mdio = Management Data Input/output	Header J1, Pin 5	Pin 41	Pin AH29
mmd_mdio_in = Management Data Input	LED D1, Green (=data rx -light)	Pin 102	Pin AK20
mmd_mdio_out = Management Data Output	LED D1, Red (=data tx -light)	Pin 104	Pin Y20
Ground for rx LED	LED D1, ground	Pin 101	Pin AG26
Ground for tx LED	LED D1, ground	Pin 103	Pin AH22

**Table 2. Pinout of the connector (MDIO)**

Table 2 shows the pinout of the connector to connect MDIO. By using the MDIO signals the user can access the registers of FES.



**Figure 18. HSMC Debug Header Breakout Board**

Figure 18 shows the HSMC Debug Header Breakout Board.

## 9 Appendix 2 Reference Design

A reference design for Altera Cyclone IV Development board is provided to make it easier for customers to start making their own FPGA designs around FES. The reference design can be downloaded from our website.

With the reference design, you can test the functionality of FES in your own application. This includes testing of IEEE1588v2 PTP (Precision Time Protocol). The reference design includes everything that is needed around FES to test its functionality, including NIOS, AFEC, and so on. No licenses are required to test the reference design.

For usage in end products Flexibilis grants Licenses for the Reference Design for free as long as it is used together with Flexibilis FES product. You can alter the reference design to fit your purposes and environment. The reference design can be compiled with Altera Quartus II tool and the resulting FPGA design can be loaded for example onto Altera Cyclone IV Development board. Instructions on how to use the Reference design can be found in this appendix. When compiling for your end product, you might need some licenses, see section 9.7.

### 9.1 Installing

Unzip the release packet containing the reference design (FESHA00E00-FBIT.zip) to a directory on your computer. To compile the design, you will also need to download the IP cores, see section 9.6.

### 9.2 Using with Quartus

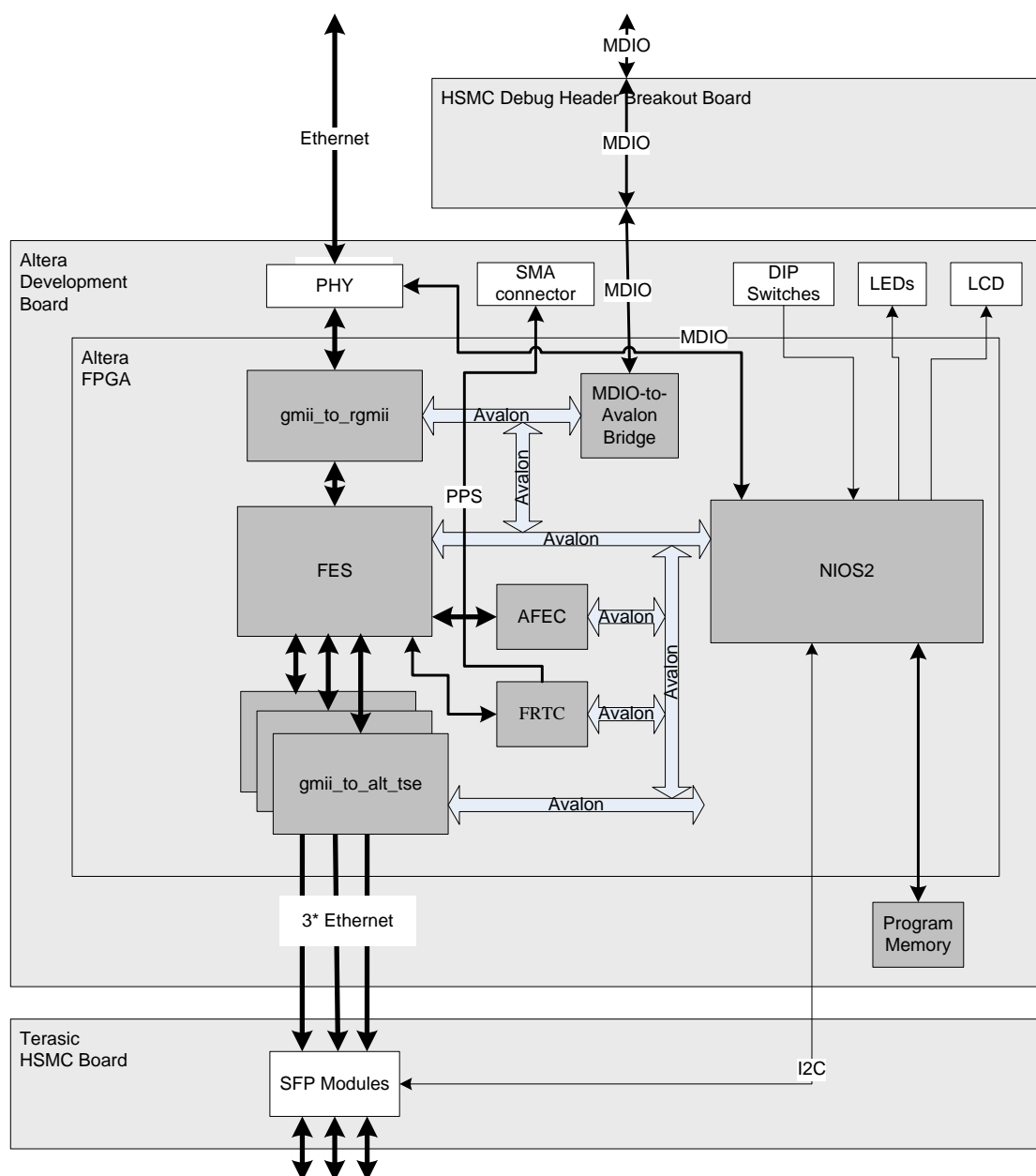
Open the Quartus II project in Quartus II by double clicking the file cyclone4GXdevkit.qpf. The top level of the design is in the file named fpga.vhd. Before the whole design can be compiled, QSYS generate has to be run first: Start by selecting Tools -> Qsys from the drop-down menu. Open xr7\_softsoc.qsys. Compile by pressing Generate button at the generate page. Compiling the whole design can then be done by selecting Processing -> Start Compilation in the Quartus II drop-down menu.

Note that the deliverables contain all the files generated by Qsys, therefore running Qsys is mandatory only when the Qsys project is changed.

### 9.3 Block Diagram

The structure of the design can be viewed with the QSYS tool. The structure of the reference design is presented in Figure 19.





**Figure 19. Reference Design Block Diagram**

## 9.4 Main Blocks

The main blocks of the FPGA reference design are FES, AFEC, FRTC, NIOS2, gmii\_to\_rgmii and gmii\_to\_alt\_tse. These are presented in the following subparagraphs.

### 9.4.1 FES

This block is encrypted so that the vhdl code cannot be viewed. It has two hour evaluation limit, after which the design stops working. FPGA reboot/reload is needed to restart the evaluation period. See FES Manual for more information on FES.

### 9.4.2 AFEC

Flexibilis Advanced Ethernet Controller (AFEC) is an Ethernet MAC IP core. This block is encrypted so that the vhdl code cannot be viewed. AFEC is needed here for NIOS2 to be able to send and receive Ethernet frames.

### 9.4.3 FRTC

Flexibilis Real-Time Clock (FRTC) provides adjustable wall clock time for FES (and AFEC). The clock time is used for IEEE 1588v2 transparent clock and frame timestamp functionality of FES. The clock time is output from FRTC also as PPS pulse, for test measurements, see Figure 19.

### 9.4.4 NIOS2 (xr7\_softsoc)

Nios II is Altera Embedded soft-core processor. The Nios II processor:

- Configures FES and the other FPGA blocks in startup and during the operation
- Controls the LCD display.
- Runs the IEEE 1588 PTP protocol stack (master and slave clock and peer-to-peer transparent clock)
- Polls the PHY chip registers and SFP modules for mode changes

Although Nios II processor is used in this design, it is not part of FES. FES can be also used without Nios II processor.

The FES IP core supports end-to-end transparent clock functionality with pure hardware and without any software assistance. The PTP protocol stack that runs on NIOS software adds the peer-to-peer transparent clock and ordinary/master clock support to the system. So, these functionalities are implemented partly with software partly with hardware. For testing purposes, the internal clock time is output as a PPS pulse to "CLKOUT" SMA connector.

### 9.4.5 gmii\_to\_rgmii

The gmii\_to\_rgmii block alters the GMII interface of FES to an RGMII interface compatible with the PHY chip on the development board.

### 9.4.6 gmii\_to\_alt\_tse

The gmii\_to\_alt\_tse block alters the GMII interface of FES to a 1000BASE-X interface compatible with SFP modules and 1000BASE-X fiber Ethernet standard when using fiber SFP modules. When copper SFP modules are used, the gmii\_to\_alt\_tse block alters the GMII interface to SGMII.

## 9.5 How to Modify the Design

Users can modify the reference design (as far as it is used together with FES). The modifying can be done for example with QSYS and NIOS II EDS tools, and the editor integrated in the Quartus II tool. The modified design can then be compiled and loaded onto Altera Cyclone IV Development board or onto some other board (requires modification of the design if the I/Os and the FPGA model are not the same).

## 9.6 How to Compile the Design and Download to the Board

To be able to compile the design, the FES, FRTC and AFEC IP cores are needed. The FES IP core can be downloaded from <http://www.altera.com/smartgrid>. Click "Request IP". To download it, you will need to enter the part number/product code FESHA00E00-FBB.

Create a directory named *encrypted\_ip* on the main level of the reference design directory (first level, in the same directory with *cyclone4GXdevkit\_softsoc*, *cyclone5GXdevkit\_softsoc* and *doc*).

Unzip the IP core packet downloaded from the Altera site. There you can find a directory named *core*. Copy the contents of this directory to the *encrypted\_ip* directory you created before.

AFEC and FRTC IP can be downloaded from Flexibilis webpage:

<http://www.flexibilis.com/products/downloads/>. Create a directory named *external* under *cyclone4GXdevkit\_softsoc* directory and *afec* and *frtc* directories under *external*. Then copy files from *afec* and *frtc* IP release *core* directories to *external/afec/* and *external/frtc/*.

Now you should be able to compile the design. If the compilation doesn't succeed, try reconfiguring the license files. In Quartus II, this can be done at **Tools -> License Setup**.

The design is compiled by selecting **Processing -> Start Compilation** from the Quartus II drop-down menu. A successful compilation will result file named *fpga/bin/cyclone4GXdevkit.sof*.

Software part of the reference design can be modified using NIOS II EDS tool. Import projects included in the reference design and create new Micrium MicroC/OS-II type NIOS II BSP. In addition, IEEE 1588 PTP stack can be licensed from us and it can be imported as a project directly to NIOS II EDS tool.

The flashing file can be created by running the script "**create\_flash\_bins.sh TSFP**" using NIOS II command line tool. This will result new *bin/fpga.flash* (and *bin/app.flash* if software is updated).

The design can then be flashed to the Altera Cyclone IV Development board by using the flashing script "**flash\_dev\_board.sh TSFP**" using NIOS II command line tool.

## 9.7 The Licenses Needed and How to Get them

Depending on your design, there are certain licensable products that might be needed in your design.

Testing with the reference design on Altera V and IV development boards doesn't require any licenses. However, when you have your own devices ready and you are compiling the binary for production, all the licenses need to be in check.

### NIOS, Altera's embedded softcore processor (Altera)

NIOS is needed only if some software (PTP Protocol stack for example) needs to be run and there is no hard CPU in the system. Flexibilis IEEE 1588 PTP Protocol stack can also be ported to other CPUs than NIOS.

NIOS can be licensed from Altera. There are two different versions available:

- IP-NIOS: just the NIOS.
- IPS-EMBEDDED: NIOS, DDR memory blocks as well as Triple-Speed Ethernet (TSE) IP. TSE is needed as SGMII/1000Base-x interface adapters.

### TSE, Triple-Speed Ethernet IP (Altera)

TSE is needed only if SGMII/1000Base-x interfaces are used. TSE is also available as an Open Core Plus (OCP) license that makes evaluation possible. With the OCP license the IP works for one hour.

Operating system, NIOS (Micrium)

NIOS operating system (uC/OS-II from Micrium) is needed only if some software (PTP Protocol stack) is running on the uC/OS-II. uC/OS-II is included in the NIOS packet, but needs to be licensed if used in products that are sold.

AFEC, Ethernet MAC (Flexibilis)

AFEC is needed only if the selected CPU doesn't have a suitable Ethernet MAC for sending and receiving Ethernet frames or if the existing Ethernet MAC lacks some required features, for example IEEE 1588 PTP support. AFEC can be licensed from Flexibilis.