FLEXIBILIS REDUNDANT SWITCH (FRS)

Altera Cyclone IV Demo

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Revision History

Rev	Date	Comments
1.0	01.02.2013	Approved version
1.1	25.02.2013	Updated FRS Reference Design packet info
1.2	18.04.2013	Minor updates (sections 4 and 11)
1.3	10.05.2013	Reference design updates
1.4	27.05.2013	Reference design updates
1.5	08.08.2013	QuadBox and IEEE 1588 demo setups added
1.6	12.02.2014	Link LED functionality changed
1.7	24.06.2014	Removed references to operating system
1.8	05.12.2014	Cut-through added. Reference design information moved to an own document. Other minor updates.
1.9	09.12.2014	Updated formatting

1 Introduction

This document contains instructions on an evaluation setup that can be used for evaluating functionality of Flexibilis Redundant Switch (FRS), an FPGA IP core from Flexibilis Oy (Inc.). Both High-availability Seamless Redundancy (HSR) and Parallel Redundancy Protocol (PRP) can be evaluated using this setup. This document is targeted for anyone who wishes to build a test setup to evaluate the functionality of FRS.

1.1 What is HSR

High-availability Seamless Redundancy (HSR) is a standard (IEC 62439-3 Clause 5) providing redundancy for Ethernet networks. HSR provides redundancy with no single point of failure and zero time to recovery in case of a failure. Single network faults in the network will not result in any frame loss. The network is fully operational during maintenance and any device can be disconnected and replaced without breaking network connectivity.

HSR is suitable for applications that require short reaction time and high availability. Originally HSR was targeted for smart grid electrical substation automation, but it can also be employed in other mission critical networking applications such as industrial automation, motion control and military communication.

Typical HSR topology is a ring (see Figure 24). The source node duplicates all the frames it has to send and sends them using two different paths to their destination. If either one of the two paths is broken, due to link failure or node failure, one copy of each frame is still able to reach the destination.

1.2 What is PRP

Parallel Redundancy Protocol is a standard (IEC 62439-3 Clause 4) to provide redundant Ethernet. Under PRP, each node is connected to two separated, parallel networks (see Figure 25). The nodes send two copies of each frame, one over each network. When a node receives a frame it accepts the first copy and discards the second, eliminating the duplicate frame.

The two networks are assumed to be fail-independent. The destination node will always receive at least one frame as long as one of the two networks is operational. This provides zero-time recovery in case of failure, so no frames are lost.

The downside of PRP is that the network cost is doubled when compared to a single non-redundant network. This makes it more expensive to implement than most of the other redundancy protocols. HSR for example provides the same level of redundancy as PRP, but with lower cost.

1.3 What is Flexibilis Redundant Switch

Flexibilis Redundant Switch (FRS) is a triple speed (10Mbps/100Mbps/1Gbps) Ethernet Layer-2 switch with HSR and PRP support. FRS in an Intellectual Property (IP) block that can be employed for example with programmable hardware (FPGA). FRS is compatible with IEC 62439-3 Clause 5 ”High-availability Seamless Redundancy (HSR)” and IEC 62439-3 Clause 4 ”Parallel Redundancy Protocol (PRP)”. Flexibilis Redundant Switch includes also IEEE1588v2 Precision Timing Protocol (PTP) end-to-end transparent clock functionality. IEEE1588 Ordinary/Boundary clock and peer-to-peer transparent clocks are implemented with hardware-software co-operation together with an attached CPU (either hardcore CPU or softcore CPU).

Flexibilis Redundant Switch IP core is available for evaluation purposes free of charge. FRS can be used to implement End-nodes and RedBoxes (For implementing a QuadBox two FRS cores are needed, but the cores can co-exist at the same FPGA). Typically one of the Ethernet interfaces of the core is internal, for the device internal CPU to be able to access the network. Typically two Ethernet ports are be used to connect to the redundant network (HSR

ring or PRP LANs) and one port is an interlink port that can be used also for maintenance purposes in case of an end-node. Figure 1 shows the typical way to use 4-port FRS.

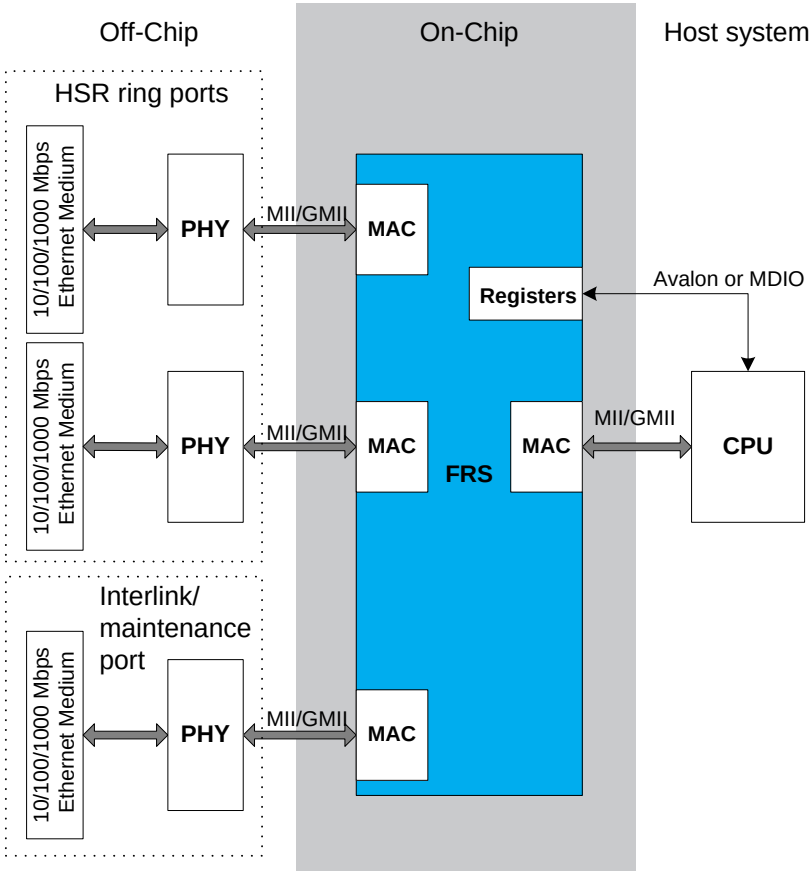

Figure 1. FRS Standard Configuration

1.4 About the test setup

This document contains instructions on constructing a simple HSR/PRP network setup between two FPGA boards and two Ethernet devices (for example laptops, see Figure 2). When only two FPGA boards are used, the setup looks exactly the same for HSR and PRP. When there are more than two boards, the setup looks different since HSR network has ring topology and PRP network has double LAN (in this case double star) topology. Sections 6 and 7 give more information on how to build a HSR or PRP network between more than two devices. QuadBox setup is presented in Chapter 8.

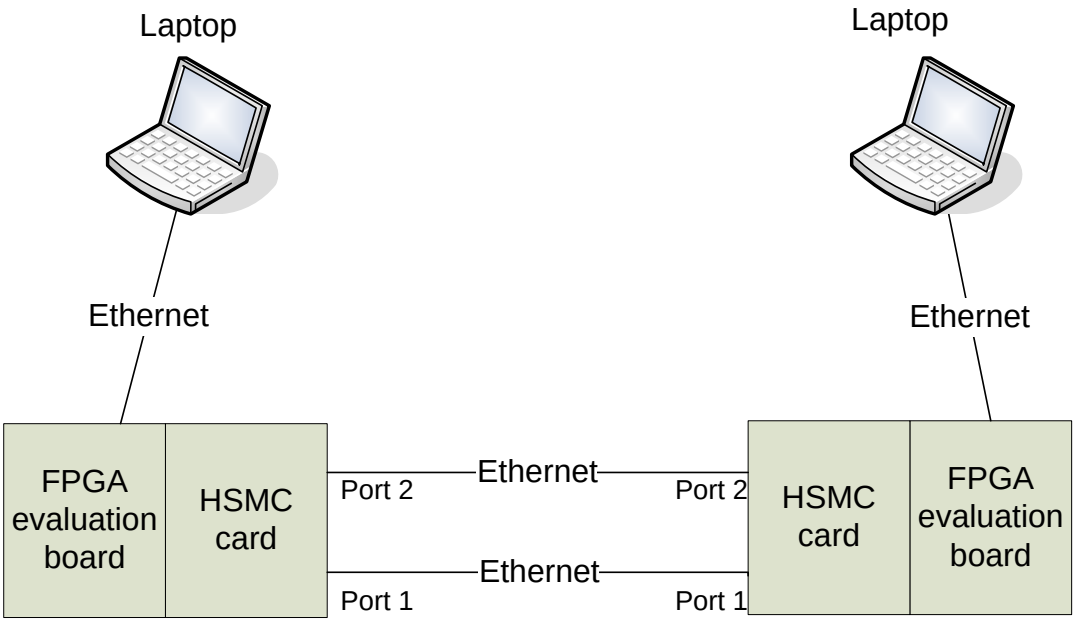

Figure 2. Structure of an Evaluation Setup for HSR and PRP

2 Equipment Needed

The following is the minimum equipment needed for building the evaluation setup (see the next page for information on where they can be ordered from).

- Two Cyclone IV GX FPGA Development Kits
- Two Terasic SFP HSMC Boards
- 4 SFP modules. They can be fiber (see Figure 3 and Figure 4) or copper SFP modules (see Figure 5) depending on what kind of cables are used (fiber or copper).
- Four Ethernet cables (fiber or copper, single or multimode)
    - At least two of them need to be copper Ethernet cables (for connecting to laptops, test equipment, webcam, etc.). All copper cables should be crossover type.
- Power adapters for the boards (comes with the evaluations boards)
- Two laptops (or other computers, or other test equipment that is able to send/receive Ethernet frames, or for example a web camera)
- USB cable for programming the boards (comes with the FPGA Development Kit)
- Six 8mm standoffs and eight 15 mm standoffs (little metal feets the board can stand on) and fourteen metal nuts (0.217"/5.51mm, M3) for the standoffs.
- Two LC-to-LC or RJ45 couplers (optional). If you use these, you will need two more Ethernet cables (fiber if using fiber cables between the boards, copper if using copper cables between the boards).

Figure 3. SFP Module for Multimode Fiber Optic Cable (Black Latch)

Figure 4. SFP Module for Single Mode Fiber Optic Cable (Blue Latch)

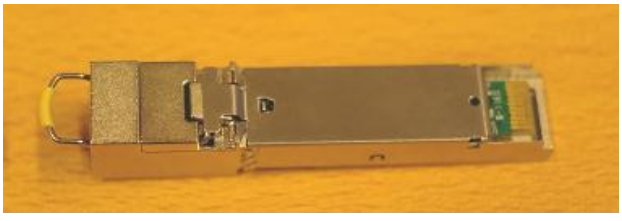

Figure 5. SFP Module for Copper Cable

Note that touching or moving the boards during operation may cause same frame loss. This is because of disturbance to the board-to-board signals. You can use LC-to-LC couplers (Figure 6) or RJ45 couplers (Figure 7) between the boards to avoid touching them while connecting or disconnecting links. If you decide to use these, you will need two more cables (six altogether).

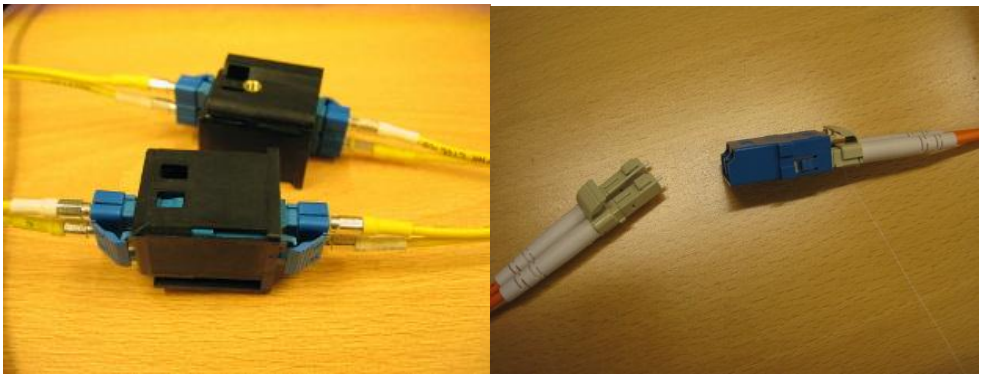

Figure 6. LC-to-LC Couplers (for Fiber Optic Cables)

Figure 7. RJ45 Coupler (for Copper Cables)

The following lists the recommended places where from the equipment needed can be ordered from:

- Cyclone IV GX FPGA Development Kit from Altera (ordering code **DK-DEV-4CGX150N)**: http://www.altera.com/products/devkits/altera/kit-cyclone-iv-gx.html
- USB cable and power adapter for the board is included in the Cyclone IV GX FPGA Development Kit.
- Terasic SFP HSMC Board: http://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&CategoryNo=71&No=342
- SFP module for multimode fiber cable from Digi-Key: http://www.digikey.com/product-search/en?x=15&y=12&lang=en&site=us&KeyWords=afbr-5715alz. Typically multimode cables are orange in color and the SFP module latch is black (see Figure 3).
- SFP module for single mode fiber cable from Digi-Key: http://www.digikey.com/product-search/en?x=15&y=12&lang=en&site=us&KeyWords=afct-5715alz. Typically single mode cable is yellow in color and the SFP module latch is blue (see Figure 4).
- SFP module for copper cable from Digi-Key: http://www.digikey.com/product-search/en?x=28&y=20&lang=en&site=us&KeyWords=FCLF-8521-3
- Single mode fiber optic cable from Digi-Key: http://www.digikey.com/product-detail/en/1435791-1/1435791-1-ND/1889887
- Multimode fiber optic cable from Digi-Key: http://www.digikey.com/product-detail/en/9-6374659-7/9-6374659-7-ND/2326175
- Copper crossover cable (RJ45) from Digi-Key: http://www.digikey.com/product-detail/en/219153-1/219153-1-ND/1892833
- LC-to-LC coupler from Digi-Key: http://www.digikey.com/product-detail/en/1828074-3/A99592-ND/1971501
- RJ45 coupler from Digi-Key: http://www.digikey.com/product-detail/en/555051-1/A9108-ND/150720

- 8 mm standoff from Digi-Key: http://www.digikey.com/product-detail/en/R30-3000802/952-1499-ND/2264480
- 15 mm standoff from Digi-Key: http://www.digikey.com/product-detail/en/R30-3001502/952-1506-ND/2264487
- 0.217" (5.51mm) M3 nuts from Digi-Key: http://www.digikey.com/product-detail/en/MHNZ%20003/H762-ND/274973

The whole packet including everything necessary for the evaluation can also be ordered from Flexibilis. Please contact contact@flexibilis.com for further information.

For the Terasic boards you may also contact local Altera distributors.

3 Software Needed

All the software mentioned here should be located on the computer that will be used for programming the boards. It can be either one of the test laptops or a third computer not connected otherwise to the HSR/PRP network.

First you'll need to have the Flexibilis Redundant Switch Reference Design packet (FESHA00E00-FBIT.zip) somewhere on the computer; the location of the file doesn't matter. If you don't yet have it, please download it from http://www.flexibilis.com/products/downloads/. In addition to the FRS programming file itself the packet also contains a Release Note and a Manual that includes more information and instructions.

Next you'll need to download and install Altera Quartus II software if you do not have it installed already. Free web edition can be downloaded at www.altera.com/support/software/download/sof-download_center.html. Figure 8 shows what the user interface of the software looks like.

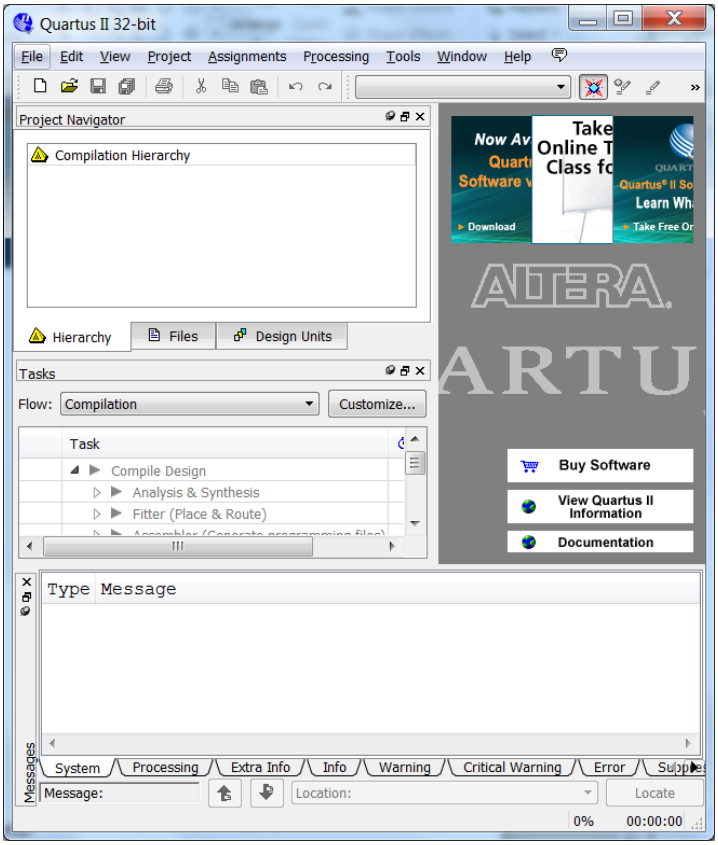

Figure 8. Altera Quartus II Software

Administrator rights are needed to be able to the install the software. Please note that installing the software might take a few hours and an Internet connection is needed for the duration of the installation process.

4 Setting up the Evaluation

If you haven't used Altera boards before, the documentation might be useful as it contains some instructions. It can be downloaded at: [www.altera.com/products/devkits/altera/kit-cyclone-iv-gx.html.](www.altera.com/products/devkits/altera/kit-cyclone-iv-gx.html)

See Figure 9 and Figure 10 for two different versions of the simple evaluation setup.

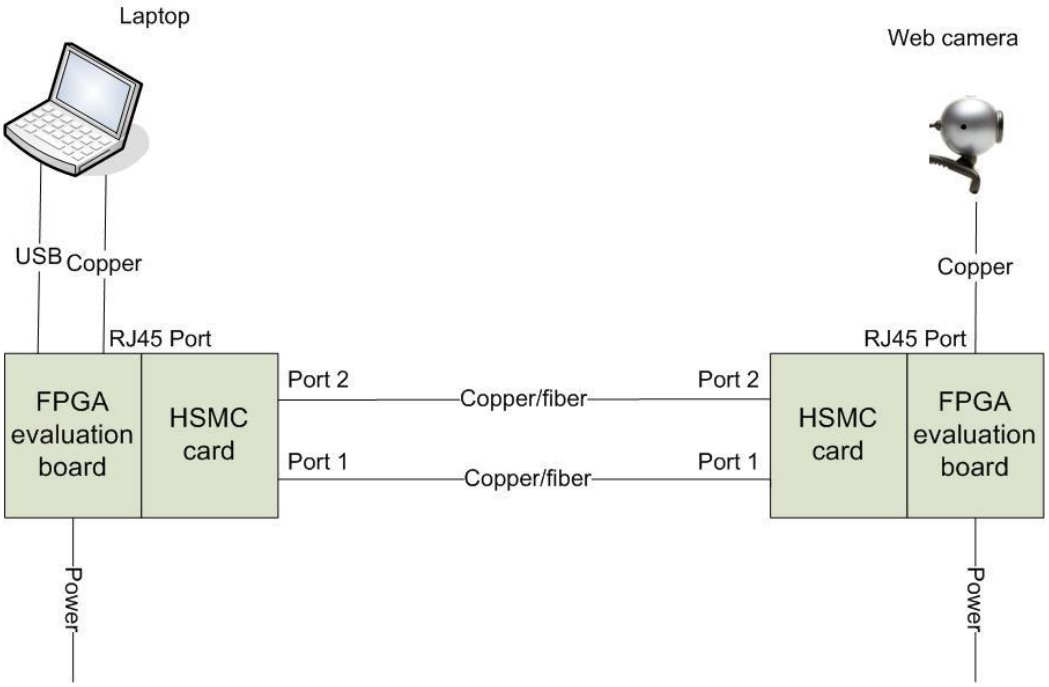

Figure 9. HSR/PRP Setup with Laptop and Web Camera

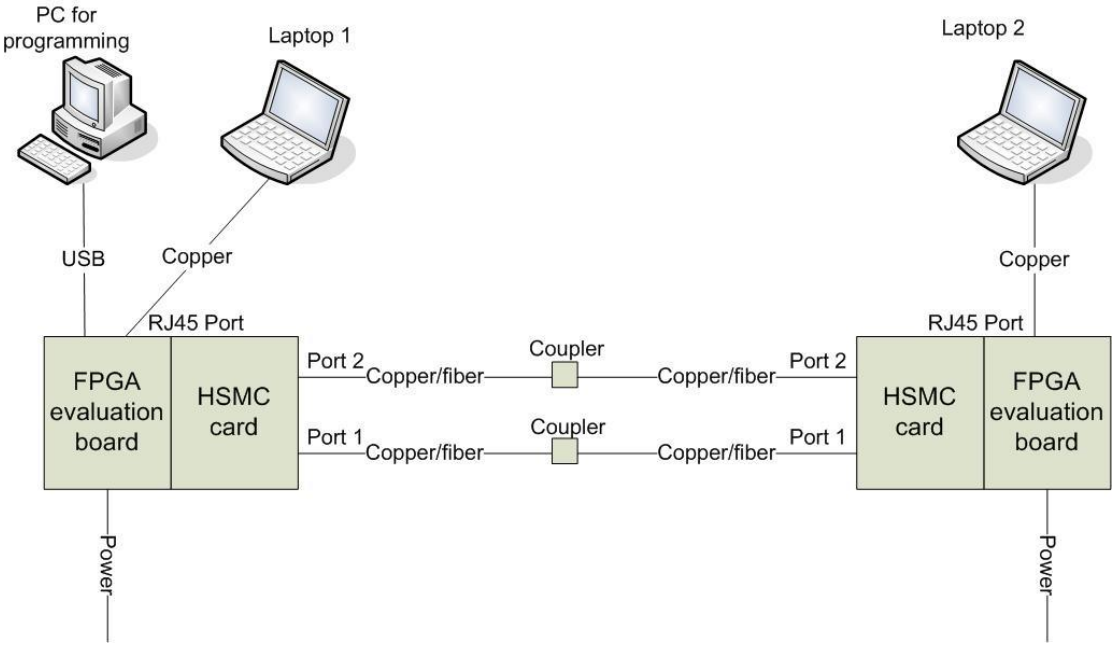

Figure 10. HSR/PRP Setup with two Laptops, PC and Couplers

4.1 Connecting the Boards Together

First you should connect the HSMC board to the FPGA board (use the HSMC A connector as presented in Figure 11). Using standoffs with the boards is recommended but not absolutely necessary (standoffs are the little metal feet the board can stand on). The 15 mm standoffs should go under the HSMC board and the 8 mm standoffs under the FPGA board. Use the nuts to tighten the standoffs to the board.

If you want to access the FPGA registers (not necessary for the evaluation), you can do this by connecting the MDIO. The MDIO can be connected with the HSMC Debug Header Breakout Board that comes with the Altera Development Kit (use HSMC B connector as in Figure 31). See Table 2 at the end of the document for the pinout of the connector. Also see www.terasic.com.tw/cgi-bin/page/archive_download.pl?Language=China&No=495&FID=6266b5c8147aac2f821702f97c440dc8 for the schematics of the board. DIP switch SW2.5 is used to select whether to enable or disable the external MDIO, see Table 1.

After connecting the FPGA board and HSMC board to each other, connect an USB cable between FPGA board and the PC used for programming. It can be either one of the test laptops or a third, separate computer.

Next, connect a power cable to the FPGA board. See Figure 11 for the setup with SFP HSMC board.

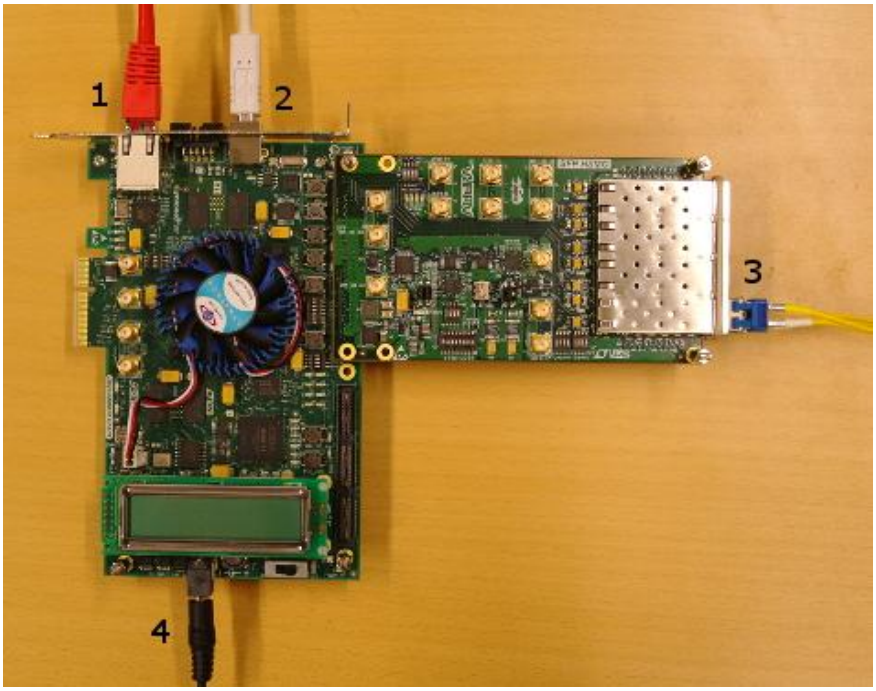

Figure 11. FPGA Connected to SFP HSMC Board

In Figure 11, number 1 is the Ethernet cable going to laptop/other device used for testing the setup. Number 2 is the USB cable used for programming, number 3 are the Ethernet cables going to the other evaluation board(s) and number 4 is the power cable.

Now, connect also the second FPGA board with the second HSMC board. See Figure 9 and Figure 10 for two alternative versions of the whole setup.

Check the onboard DIP switches on both FPGA boards. The DIP switch SW2.1 is used to select whether FRS is working as a HSR RedBox or as a PRP RedBox. This setting can be changed later, so at this point it doesn't matter whether you choose HSR or PRP.

DIP switch settings for SW1 (see Figure 12):

- SW1.1 USER_FACTORY "ON" ("0")

- SW1.2 CLK125_EN “OFF” (“1”)
- SW1.3 CLKA_EN “OFF” (“1”)
- SW1.4 CLK_SEL “ON” (“0”)

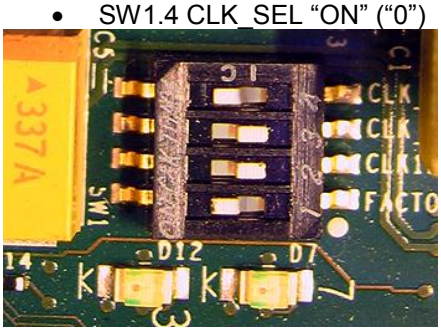

Figure 12. DIP Switch SW1 Settings

DIP switch SW2 settings for HSR Redbox (see Figure 13):

- SW2.1 “OFF” (“1”)
- SW2.2 “ON” (“0”)
- SW2.3 “any” (“0” or “1”)
- SW2.4 “OFF” (“1”)
- SW2.5 “ON” (“0”)
- SW2.6 “any” (“0” or “1”)
- SW2.7 “any” (“0” or “1”)
- SW2.8 “ON” (“0”) (reserved switch)

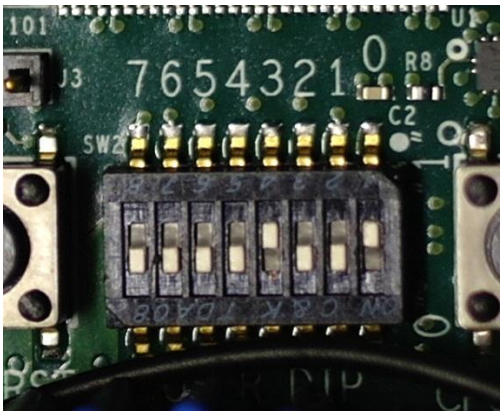

Figure 13. DIP Switch SW2 Settings for HSR RedBox

DIP switch SW2 settings for PRP RedBox (see Figure 14):

- SW2.1 “ON” (“0”)
- SW2.2 “ON” (“0”)
- SW2.3 “any” (“0” or “1”)
- SW2.4 “OFF” (“1”)
- SW2.5 “ON” (“0”)
- SW2.6 “any” (“0” or “1”)
- SW2.7 “any” (“0” or “1”)
- SW2.8 “ON” (“0”) (reserved switch)

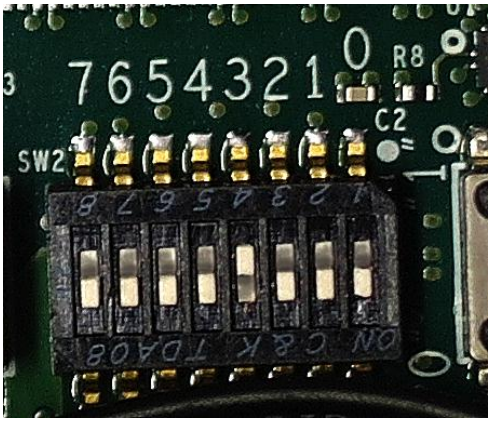

Figure 14. DIP Switch 2 Settings for PRP RedBox

The position of the switches not seen in the two Figures above (SW4 and SW5) doesn't matter; they can be at their default settings. SW3 is the power switch (on/off). For more information on the DIP switches you can check the documentation of the development board (www.altera.com/products/devkits/altera/kit-cyclone-iv-gx.html). Also see Table 1 that presents the usage of SW2 switches.

Switch (as presented in Altera documentation)	Usage	Printed on the DIP switch component	Printed on the circuit board
SW2.1	Selects the mode for redundant ports (port 1 and port 2) ON: Redundant ports are in PRP mode OFF: Redundant ports are in HSR mode This selection is valid only when SW2.2 is ON.	1	0
SW2.2	ON: Flexibilis Redundant Switch (FRS), ports 1 and 2 are in PRP or HSR mode, depending on SW2.1 OFF: Flexibilis Ethernet Switch (FES), all ports are normal Ethernet	2	1
SW2.3	ON: port 3 is in PRP interlink mode OFF: port3 is in HSR interlink mode This selection is valid only when both SW2.2 and SW2.4 are ON.	3	2
SW2.4	Selects the mode for port 3 (together with SW2.3). ON: port 3 is in PRP or HSR interlink mode (depending on SW2.3) OFF: port3 is in normal (non-HSR, non-PRP) Interlink mode.	4	3

	This selection is valid only when SW2.2 is ON.		
SW2.5	ON: Normal mode. The internal NIOS processor accesses the registers of FRS. Do not use the external MDIO interface. OFF: The internal NIOS processor won't access FRS registers. The external MDIO can be used to access FRS registers.	5	4
SW2.6	This DIP selects the PRP NetId for the attached PRP network. Only valid when configured into PRP interlink mode (SW2.3 and SW2.4). ON: NetId = 1 OFF: NetId = 2	6	5
SW2.7	Selects Cut-Through or Store-Forward operation between ring ports when in HSR RedBox mode with non-HSR non-PRP interlink. In other modes the operation is always Store-Forward independent of this setting. ON: Cut-Through OFF: Store-Forward	7	6
SW2.8	Reserved for future use.	8	7

Table 1. Usage of the SW2 DIP Switches

Independent of the dip switch settings the mode of the port 4 is always normal (non-HSR, non-PRP) Ethernet (Interlink).

The SFP HSMC board DIP switches can be left at their default position, see Figure 15 for reference.

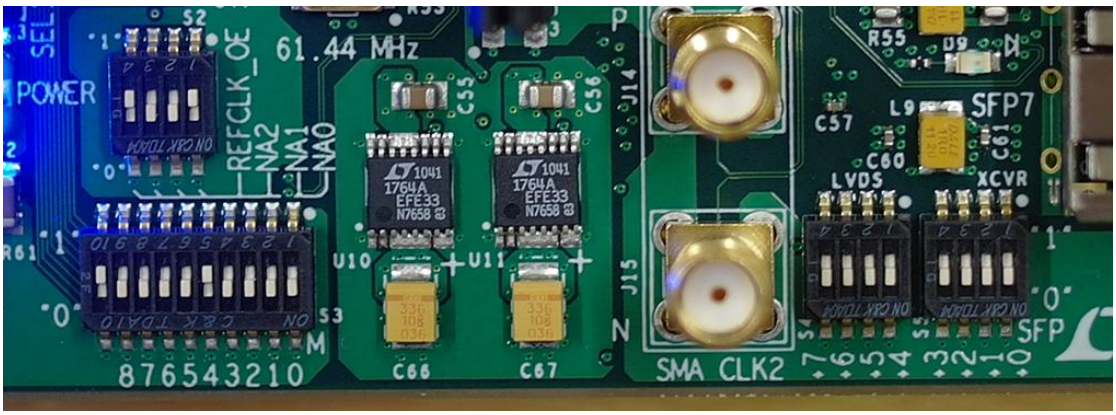

Figure 15. SFP HSMC Board DIP Settings

To save some space, the boards can be piled on top of each other with the help of standoffs. See Figure 16 for reference.

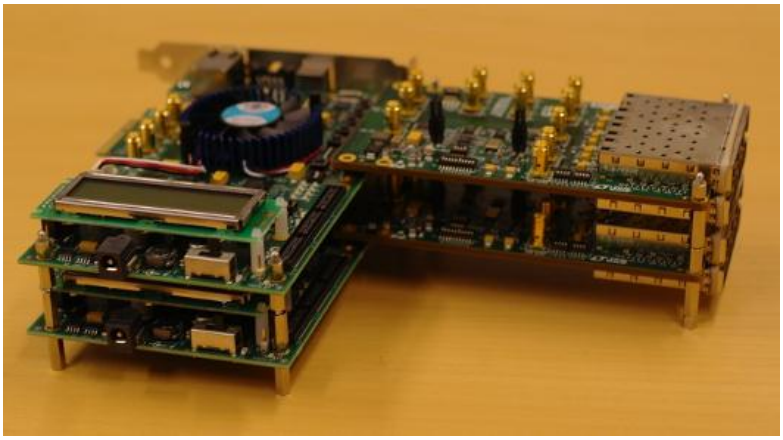

Figure 16. Boards Piled Up

4.2 Connecting the Cables

Figure 17 shows the SFP HSMC board port numbering.

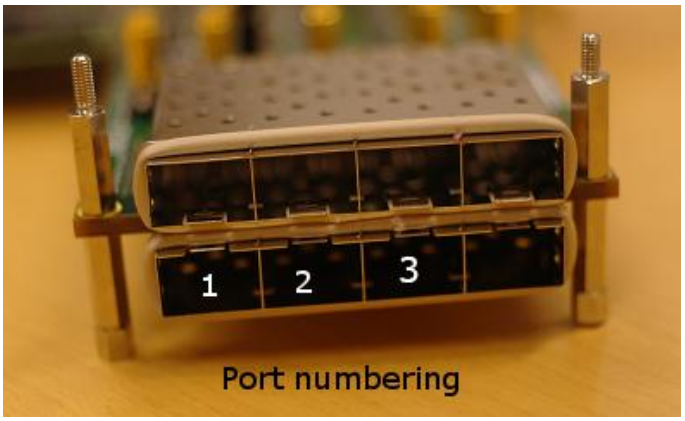

Figure 17. Port Numbering of SFP HSMC Board

Attach an Ethernet cable from the first board port 1 to the second board port 1. To be able to attach the cables to the SFP board you need to use the SFP modules. Also, remember to put the coupler between if you intend to use couplers. Then attach a cable from port 2 to port 2.

Install an Ethernet cable from the first laptop to the first FPGA board (RJ45 port) and do the same for the second laptop and second board. You can replace the laptops with any other Ethernet devices. See Figure 9 and Figure 10 for two alternative versions of the setup.

4.3 Configuring the FPGA Boards

Turn on the Altera boards. Unzip/extract the FRS Reference Design packet (FESHA00E00-FBIT.zip) somewhere on the computer used for programming if you haven't done so already. Then open the NIOS command prompt, located at somewhere like **Start** -> **All Programs** -> **Altera** -> **Nios II EDS 13.0** -> **Nios II 13.0 Command Shell**.

The FRS packet contains a folder named "cyclone4GXdevkit_softsoc" and under that there is a folder named "script". You have to change to this "script"-directory in the command shell. You can move from one directory to another with the command **cd**. To get to the Windows hard drive root directory you should write **/cygdrive** at the beginning.

For example, if the FRS packet was extracted to C:\users\you\downloads\FESHA00E00-FBIT, type

cd /cygdrive/c/users/you/downloads/FESHA00E00-FBIT/cyclone4GXdevkit_softsoc/script

Command **pwd** shows in which directory you are in right now. So now if you type **pwd** and press enter, it should show you “/cygdrive/c/users/you/downloads/FESHA00E00-FBIT/ cyclone4GXdevkit_softsoc /script”.

Run the flashing script by typing **./flash_dev_board.sh TSFP** . This will load FRS to the flash memory at the FPGA board.

Wait for the script to finish. This can take for about 10 minutes. After it has finished, unplug the USB cable from the FPGA board and connect it to the second board. Now type **./flash_dev_board.sh TSFP** again in the command prompt to run the script also for the other board. If you have more than two boards, repeat the process for all of them.

After you have run the flashing script for all the boards, turn them off. Then turn them on again. Now the FPGA program should load itself from the Flash memory to the FPGA

If the LCD Screen shows “Mode: HSR Redbox” or “Mode: PRP Redbox”, the program has been loaded from the Flash memory to the FPGA correctly. If not, you have to load the user configuration from the Flash memory at the board to the FPGA chip using the pushbuttons. You can do this by first pressing PGM_SEL button. With the button you can go through and select between three alternatives, select “USER” (the LED above text “USER” is on). Then press PGM_LOAD once to load the user configuration. See Figure 18 or Altera Manual for reference.

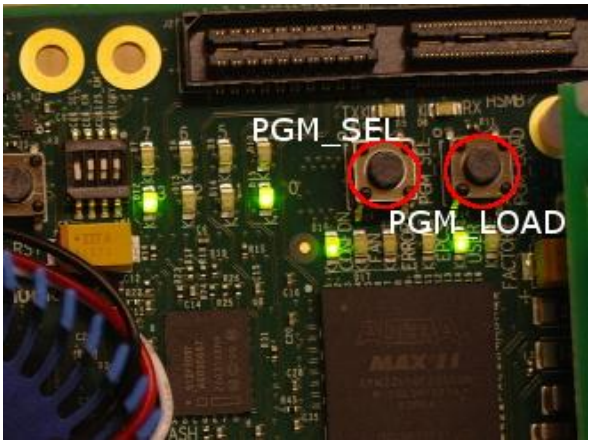

Figure 18. PGM_SEL and PGM_LOAD Buttons

Check the LEDs: if you are using HSR, LED number 7 should be on and 0 should be flashing (see Figure 19). If you are using PRP, LED number 3 should be on and 0 should be flashing (see Figure 20). LEDs number 1, 2 and 4-6 are for internal use and might be on or flashing sometimes too.

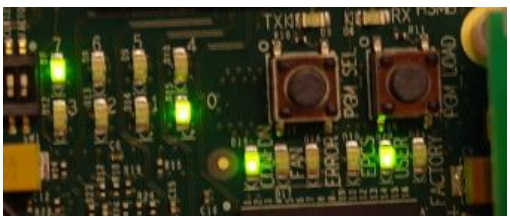

Figure 19. LEDs When Using HSR

Figure 20. LEDs When Using PRP

4.4 Configuring IP Addresses

The laptops or other devices connected to the HSR/PRP network should be in the same IP subnetwork. When subnet mask is 255.255.255.0 the computers are in the same subnetwork if the first three parts of the address are the same and only the numbers after the last dot are different. This is the case for example with IP addresses 192.168.0.1 and 192.168.0.2.

To use the HSR/PRP network, a static IP address should be defined for all the devices. In Windows 7, this can be done at **Start** –> **Control Panel** -> **Network and Internet** -> **Network and Sharing Center** -> **Change adapter settings** -> **Local Area Connection** -> **Properties** -> **Internet Protocol Version 4** -> **Use the following IP address**. Administrator rights are needed to be able to change the IP address.

You can change the IP addresses for example to 192.168.0.1 (the first laptop), 192.168.0.2 (the second laptop) and the subnet mask to 255.255.255.0 for both laptops. If you are using some other device, like a web camera, check from its instruction manual how to change its IP address, or you can check its default IP address from the manual and change only the IP addresses of the laptops so that they are in the same subnetwork.

In Windows 7, the current IP address of the computer can be checked at **Start** -> **All Programs** -> **Accessories** -> **Command prompt**. Type **ipconfig** and press enter. This will show you all the IP addresses of the computer. Search for the line that says “Ethernet adapter Local Area Connection” and under that you can see the IPv4 address and subnet mask (see Figure 21).

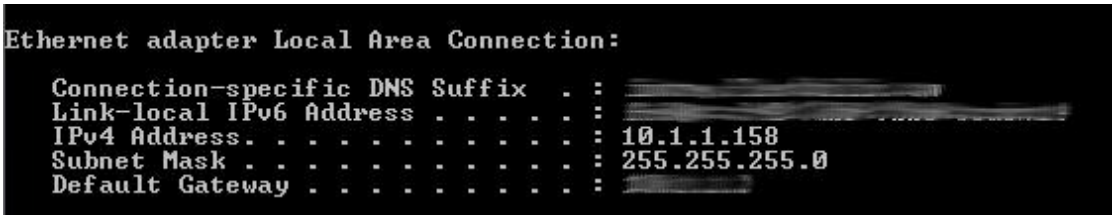

Figure 21. Checking the IPv4 Address

5 Testing

5.1 Testing the connection

At this point your setup is ready to be tested. This can be done by transferring traffic of some sort, for example by FTP if you have FTP server and client installed. Another possibility is to ping from one laptop to another.

In Windows 7, you can ping another computer or other device by first opening the command prompt (**Start** -> **All Programs** -> **Accessories** -> **Command prompt**). Type **ping** and the IP address you are trying to connect to (for example **ping 192.168.0.2**) and press enter. Figure 22 shows how the response looks like if everything works correctly.

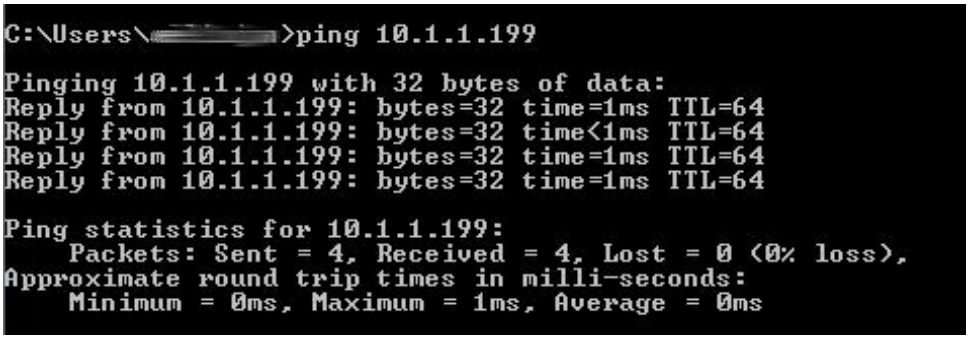

Figure 22. Ping Is Working

By typing **ping 192.168.0.2 –t** you can ping until **CTRL+C** is pressed. During the file transfer/ping you can disconnect either one of the PRP/HSR links without disturbing the file transfer/ping. Remember to disconnect using the LC or RJ45 couplers. Touching the boards can cause frame loss. Now you can check from the ping output that there was no packet loss.

You can change from HSR mode to PRP mode and other way around by first shutting down the boards. Then set DIP switch SW2.1 to OFF (1) for HSR or to ON (0) for PRP, as instructed in section 4. Then turn the boards back on and load the user FPGA configuration using PGM_SEL and PGM_LOAD buttons as instructed in section 4.3.

There is a time limit of **2 hours** for the evaluation. After the time runs out, the boards stop working. If this happens, just turn off the boards and then turn them on again. This will reset the FPGA and it starts counting the evaluation period from the beginning. Every time you shut down the boards and turn them on again, you may need to load the user configuration by pressing PGM_SEL and then PGM_LOAD.

After FRS has been programmed to the flash memory of the board once, there is no need to do it again except when upgrading to a newer version. FRS needs to be reprogrammed to the Flash again also if some other configuration file was programmed to the FPGA board user configuration.

5.2 LCD Display

The LCD display of the FPGA board shows the status of the board and the Ethernet interfaces. There are six different views. The view can be changed with the PB0 –button on the Altera board (see Figure 23). It is the fourth button counted from the PCIe back plate (if installed).

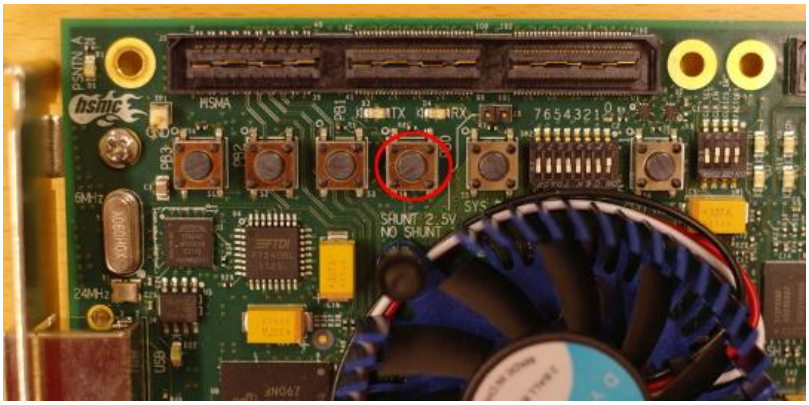

Figure 23. PB0 –button to change the screen view

5.2.1 First view

The first view tells the mode the FPGA board is currently on. It can look for example like this:

MODE: HSR RedBox
For Terasic SFP

The different options for the first line are “HSR Redbox”, “HSR(C) Redbox”, “PRP Redbox”, “FES”, “HSR-HSR RB”, “HSR-PRP R1” and “HSR-PRP R2” depending on the dip switch settings. (see chapter 4.1).

5.2.2 Second view

The second view shows the version numbers of the FRS IP core (the first line) and the version numbers of the reference design currently on the board (the second line). It can look for example like this:

IP: 2.3.2 17037
REF: 1.1 17048

5.2.3 Third view

The third view shows the interface speed on each port. P0 means the internal port used by NIOS softcore CPU. P1 is SFP port 1, P2 is SFP port 2 and P3 is SFP port 3 as indicated in Figure 17. P4 is the RJ45 (Ethernet port) on the FPGA board. The view can look for example like this:

P0: Force 100
P1: Autoneg 1000
P2: Autoneg 1000
P3: Link down
P4: Autoneg 100

The different options for port modes are “Autoneg 1000”, “Autoneg 100”, “Autoneg 10” and “Link down”. CPU port is always “Force 100”

5.2.4 Fourth view

The fourth view can look for example like this:

P0 TX 14623
P0 RX 14623
P1 TX 29246
P1 RX 14623
P2 TX 29246
P2 RX 14623

P3 TX 0
P3 RX 0
P4 TX 0
P4 RX 0

The numbers after TX and RX indicate how many packets have been received from and transmitted to each port. P0 means the internal port used by NIOS. P1 is SFP port 1, P2 is SFP port 2 and P3 is SFP port 3 as indicated in Figure 17. P4 is the RJ45 Ethernet port on the FPGA board.

5.2.5 Fifth view

The fifth view tells how many frames with errors in them have been received and transmitted. OW means an overflow: it indicates that there has been too much traffic compared to the capacity of the link. Please note that the link capacity of the HSR and PRP ports is a little bit lower than the capacity of the normal Ethernet ports because of the overhead caused by the extra header.

P0 TXE 0 RXE 0
P0 OW 0
P1 TXE 0 RXE 0
P1 OW 0
P2 TXE 0 RXE 0
P2 OW 0
P3 TXE 0 RXE 0
P3 OW 0
P4 TXE 0 RXE 0
P4 OW 0

P0 means the internal port used by NIOS. P1 is SFP port 1, P2 is SFP port 2 and P3 is SFP port 3 as indicated in Figure 17. P4 is the RJ45 Ethernet port on the FPGA board.

5.2.6 Sixth view

The sixth view tells the IEEE 1588 PTP synchronization status. OffM means the offset from the master clock in nanoseconds and P0, P1, P2, P3 indicate measured P2P mode peer delay in nanoseconds.

OffM: 15

P0: 319

P1: 312

P2: 0

P3: 0

6 HSR with Three or More Boards

HSR is typically used with ring topology. Any link in the ring can be disconnected during the operation without interrupting the traffic. A board can be turned off without interrupting the traffic of other nodes in the ring. For example in Figure 24 the board that has no laptop connected can be turned off without interrupting the traffic between the laptops.

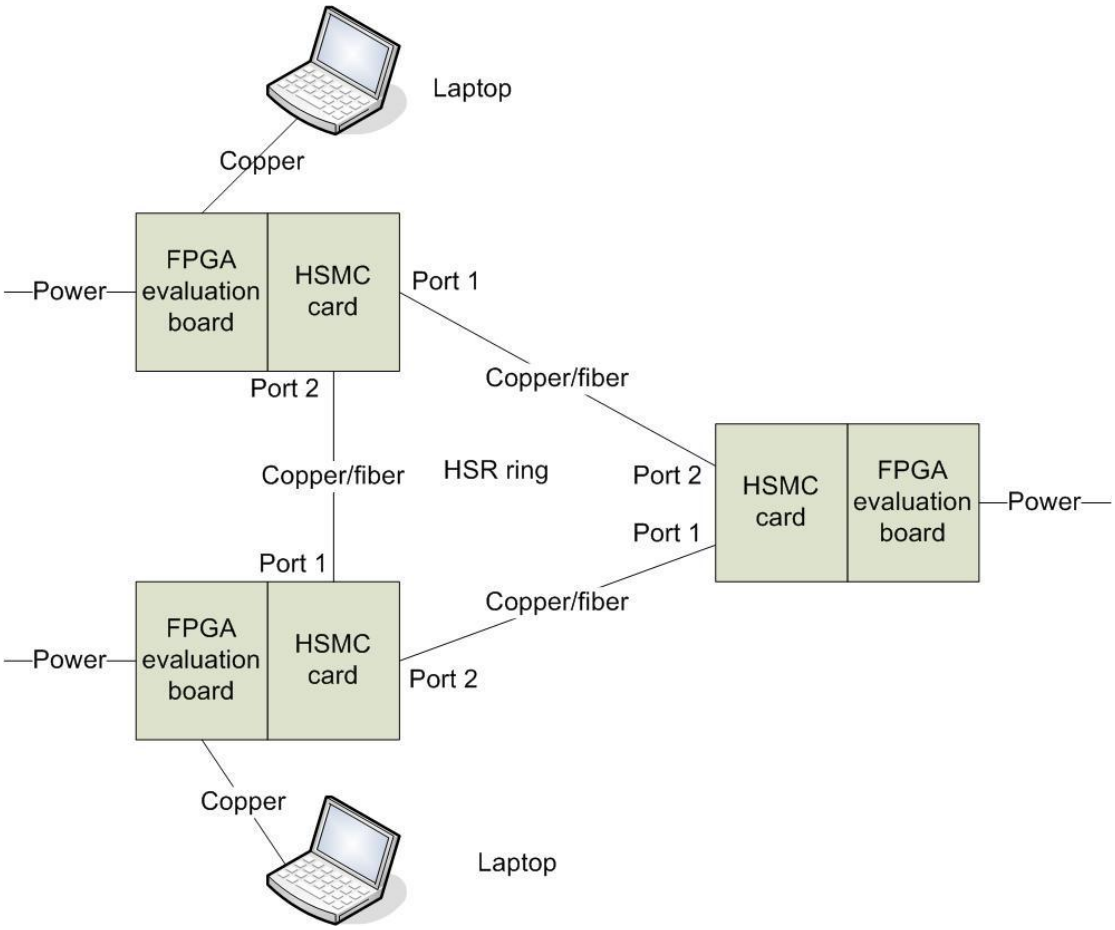

Figure 24. HSR Ring between Two Laptops

Note that the HSR ring consists of links connected to ports 1 and 2. The test devices (for example laptops) can be connected either to port 3 (SFP) or to port 4 (RJ-45).

7 PRP with Three or More Boards and with Ethernet Switches

PRP is typically used with double LAN topology (not a ring). Normal (non-PRP-aware) Ethernet switches can be used in LAN_A and LAN_B. Any link can be disconnected during the operation without interrupting the traffic. Also, either one of the Ethernet switches can be turned off without interrupting the traffic. See Figure 25 for reference.

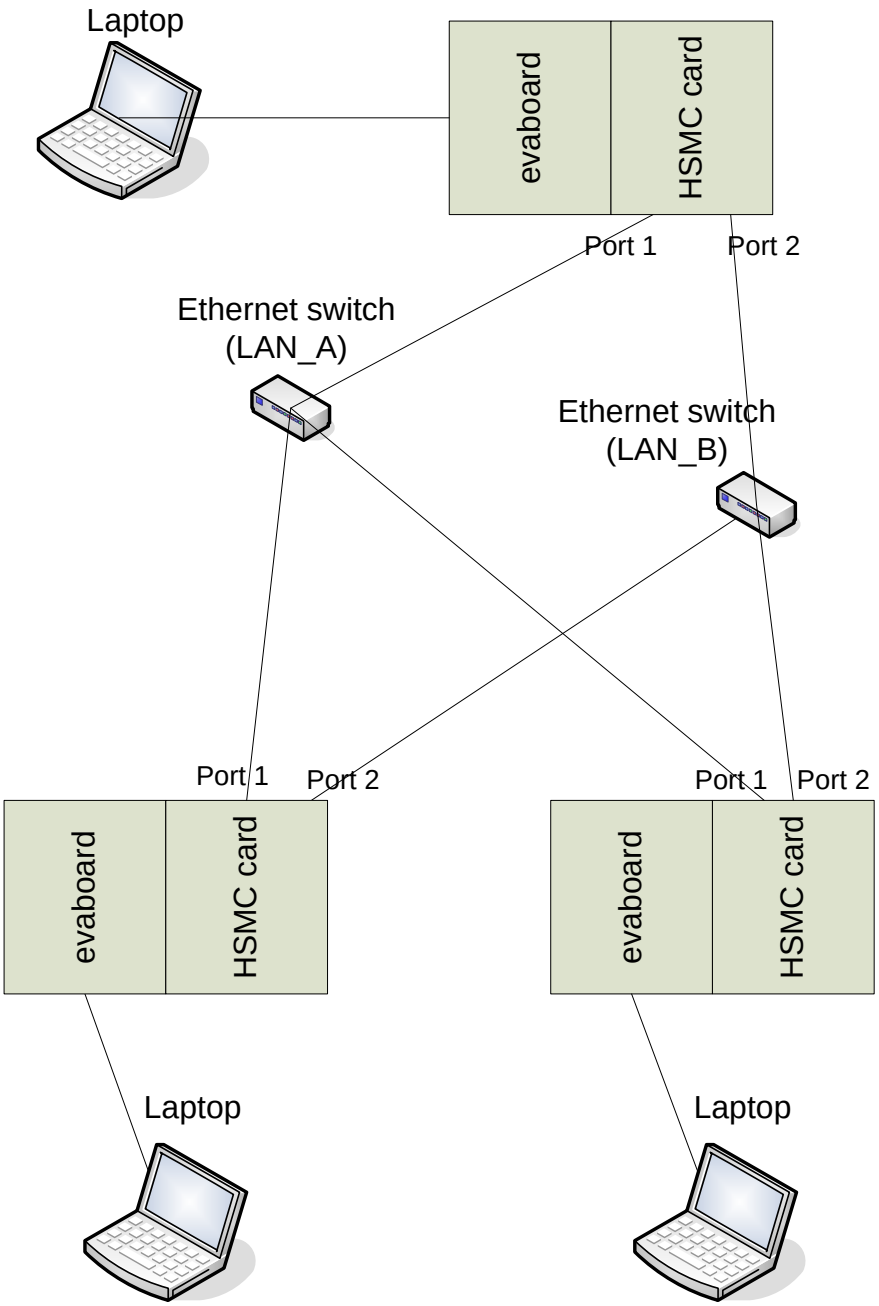

Figure 25. PRP Setup with Three Boards

8 QuadBox Test Setup

A QuadBox connects an HSR ring to another HSR ring. Typically two QuadBoxes are used between rings, to remove the single point of failure only one QuadBox would cause. A QuadBox can be constructed using two FRS IP cores. In the end product the two FRS cores can be located on the same FPGA chip. In this demo two Altera boards (one FRS core on each board) are used to form a QuadBox, as presented in Figure 26. The boards acting as half-QuadBoxes are configured as HSR-HSR RedBoxes. This means that their interlink port that connects to the other half-QuadBox is in HSR mode. Configure port 3 to HSR interlink mode using the DIP switches (see Table 1). When correctly configured the LCD display of the half-QuadBox says “MODE: HSR-HSR RB”.

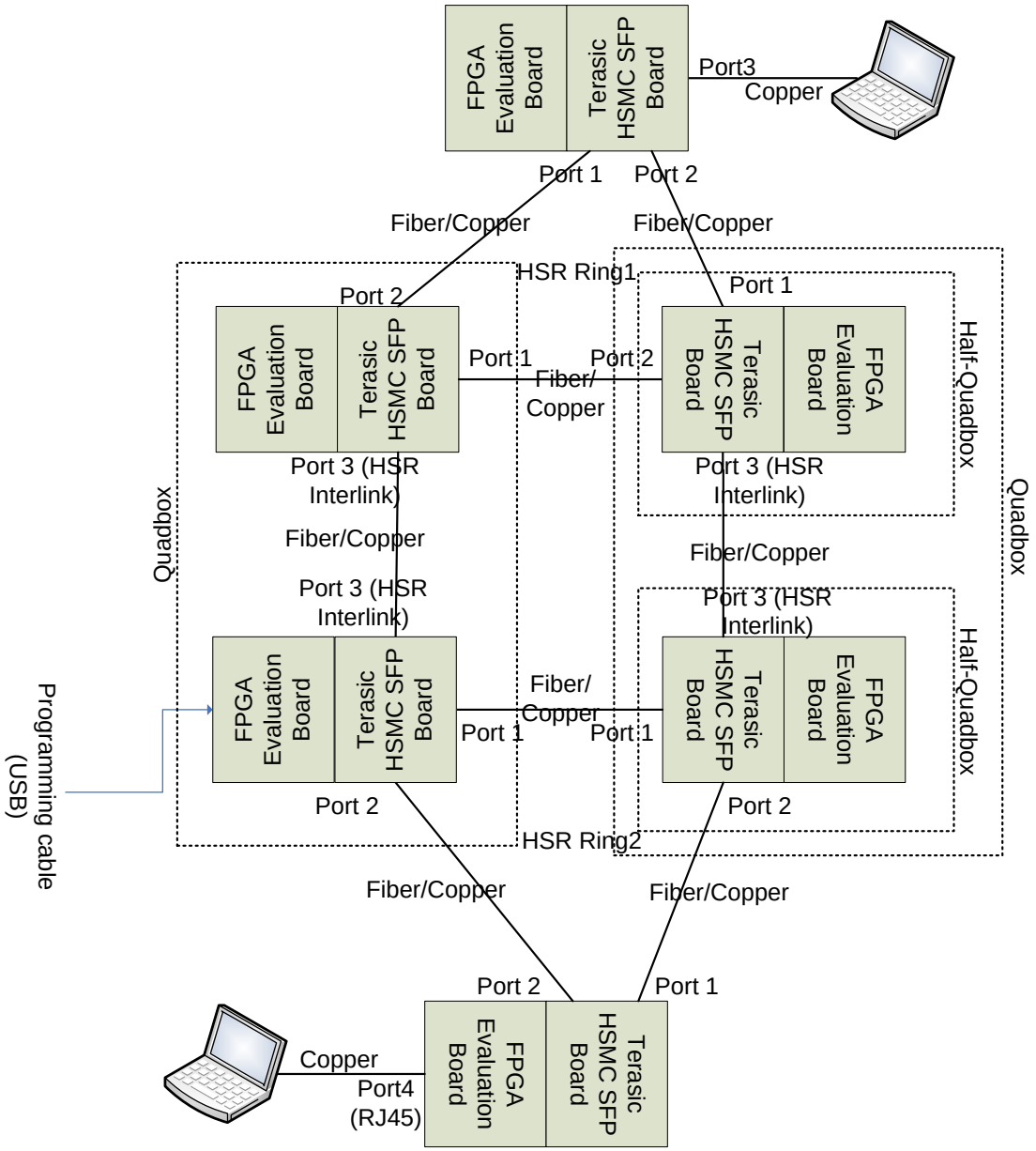

Figure 26. QuadBox Test Setup

9 IEEE 1588 Test Setup

The IEEE 1588 functionality of FRS can be tested with the setup presented in Figure 27. In the Figure 27 there is a HSR ring with four nodes, but this is just an example; the IEEE 1588 functionality can be tested with any network topology, HSR or PRP.

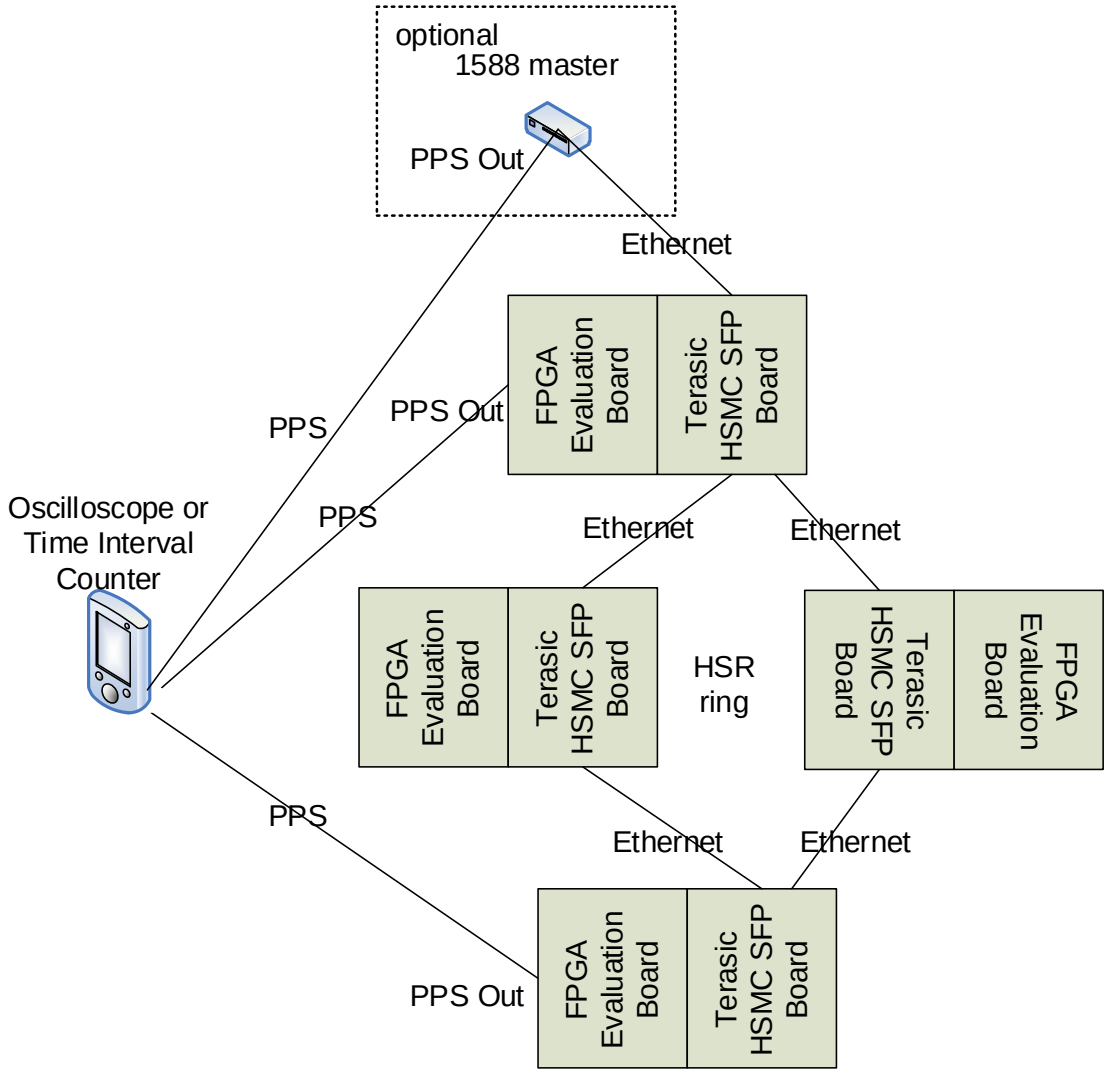

Figure 27. IEEE 1588 Test Setup

The evaluation board supports IEEE 1588 Master Clock functionality, IEEE 1588 Slave Clock functionality and IEEE 1588 Transparent Clock functionality. The Master Clock is selected automatically by the Best Master Clock algorithm. If a third party Master Clock is present it will be selected as Master Clock, and the evaluation boards will be slaves. The evaluation boards are also transparent clocks at the same time. The transparent clock functionality works between all the ports, not just the ring ports.

From the sixth view of the LCD display (see Chapter 5.2) you can see the calculated offset from the master clock and the peer nodes. The LCD display of the Master Clock says “Master”).

An oscilloscope (or time interval counter) can be connected to the PPS outputs of the boards to see the clock time difference between the boards. The PPS output is the SMA connector J9. There is text “CLKOUT” next to the connector.

The 1588 settings of the Altera demo board are according to the 1588 Power Profile: The priority is 128 and the transparent clock mode is peer-to-peer (not end-to-end). In FRS and in the software these settings are configurable but in the current demo setup these settings cannot be changed.

10 Troubleshooting

10.1 Programming Hardware Cable Not Detected

- Check the USB cable between the programmer PC and evaluation board
- Check the POWER LED on the Altera board
- Check the USB_DISABLE switch on the board (USB should not be disabled)
- Change the programming cable number in the file named ”environ” (can be found from the FRS packet, script –folder. The file can be opened with a text editor), line 20, try:
    - CABLE="--cable=0”
    - CABLE="--cable=1”
    - CABLE="--cable=2"

10.2 Link Does Not Go Up

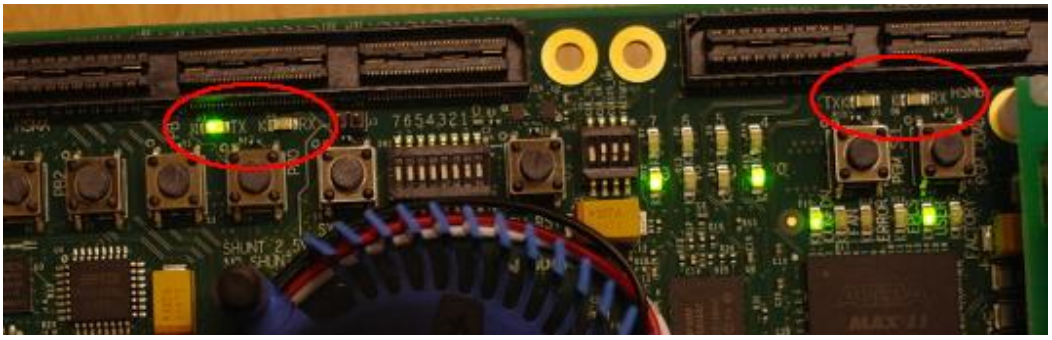

Figure 28. Red Circles Indicate the Four Link LEDs

Figure 28 shows the LEDs that indicate if the link is up or not. The LEDs and the corresponding links are:

D4: HSMCA_RX: Port 1 (see Figure 17)
D3: HSMCA_TX: Port 2 (see Figure 17)
D6: HSMCB_RX: Port 3 (see Figure 17)
D5: HSMCB_TX: Port 4 (RJ45 port at the FPGA board)

The LCD display is presented in section 5.2.

Also computers and other Ethernet devices typically have link LEDs. They are usually located next to the Ethernet port and they should be on when the link is up.

If the link LED is not on even though it should be:

- Check that all the cables are properly attached, the FPGA board and SFP board are properly attached to each other’s and that the boards are switched on
- Check that the fiber optic modules and the cables are of the same type
    - Single mode fiber is typically yellow and it should be used only with single mode modules who typically have blue latches, see Figure 4
    - Multimode fiber is typically orange in color and it should be used only with multimode modules who typically have black latches, see Figure 3
- The copper cable has to be the crossover type, so check the cable type. Crossover cable (see Figure 29) has different pinouts at each end, which means that the colored lines (wires) you can see through the plastic at the end of the cable (green, blue, red) are in different order at different ends of the cable. On the other hand, straight cables have the same pinout on both ends. You can see this in Figure 30: on both ends the colored lines at the end of the cable are in order green – blue – red.

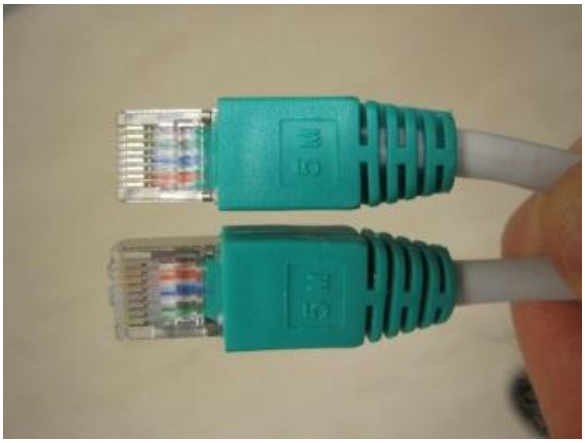

Figure 29. Crossover Cable

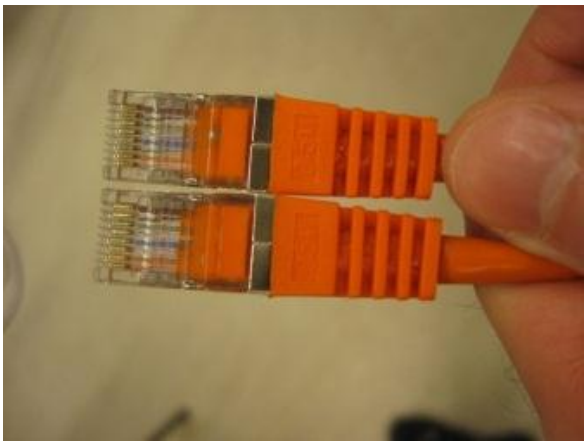

Figure 30. Straight Cable

10.3 File Transfer/Ping Does Not Work

- Check that all the links are up!
- Check the IP addresses: are the computers in the same subnetwork or is there something else wrong with the addresses? See section 4.4 Configuring IP Addresses how to define the IP addresses
- Check that file transfer/ping works with a straight cable connection between the laptops (connect the two laptops to each other's with a crossover copper cable)
- Check the firewall settings of the laptops. Try disabling the firewall and see if file transfer/ping starts working
- There is a time limit of 2 hours for the evaluation. If this time runs out the network will stop working. To get it to working again, turn off the boards and then turn them on again and load the user program.

11 Known Issues

Automatic loading of the user configuration might not be working if the FPGA board has an old version of the CPLD code. Follow Altera instructions on how to update the CPLD configuration if automatic loading of the user configuration at startup is needed.

12 Appendix 1 External MDIO

Signal	HSMC Debug Header Breakout Board	HSMC connector B	FPGA
mmd_mdc = Management Data Clock	Header J1, Pin 29	Pin 79	Pin AE25
mmd_mdio = Management Data Input/output	Header J1, Pin 27	Pin 77	Pin AE26

Table 2. Pinout of the connector (MDIO)

Table 2 shows the pinout of the connector to connect MDIO. By using the MDIO signals the user can access the registers of FRS.

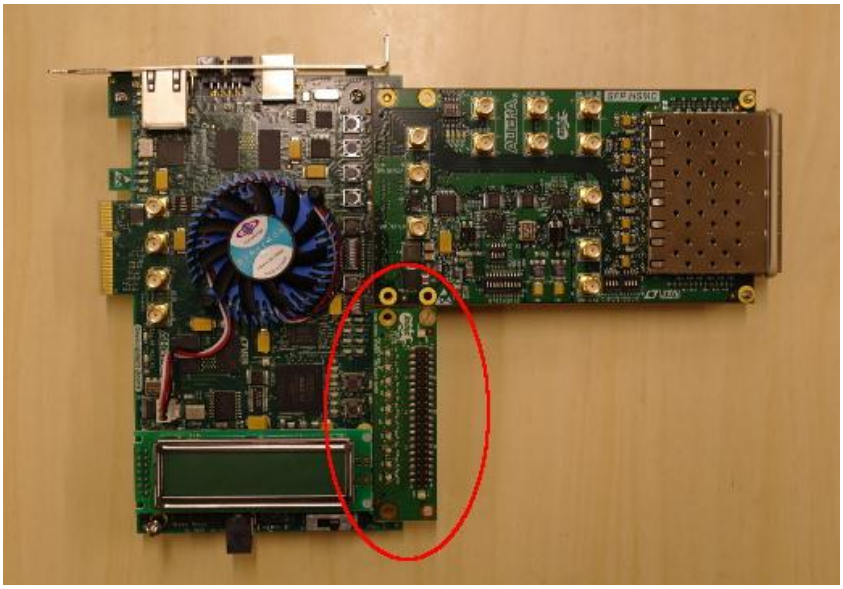

Figure 31. HSMC Debug Header Breakout Board

Figure 31 shows the HSMC Debug Header Breakout Board.