FLEXIBILIS REDUNDANT SWITCH (FRS)

Terasic SoCkit Demo

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Revision History

Rev	Date	Comments
1.0	25.8.2015	First release
1.1	5.11.2015	Added SW6 information

1 Introduction

This document contains instructions on an evaluation setup that can be used for evaluating functionality of Flexibilis Redundant Switch (FRS), an FPGA IP core from Flexibilis Oy (Inc.). Both High-availability Seamless Redundancy (HSR) and Parallel Redundancy Protocol (PRP) can be evaluated using this setup, as well as normal Flexibilis Ethernet Switch (FES). This document is targeted for anyone who wishes to build a test setup to evaluate the functionality of FRS.

1.1 What is HSR

High-availability Seamless Redundancy (HSR) is a standard (IEC 62439-3 Clause 5) providing redundancy for Ethernet networks. HSR provides redundancy with no single point of failure and zero time to recovery in case of a failure. Single network faults in the network will not result in any frame loss. The network is fully operational during maintenance as any device can be disconnected and replaced without breaking network connectivity.

HSR is suitable for applications that require short reaction time and high availability. Originally HSR was targeted for smart grid electrical substation automation, but it can also be employed in other critical networking applications such as industrial automation, motion control and military communication.

Typical HSR topology is a ring (see Figure 23). The source node duplicates all the frames it has to send and sends them using two different paths to their destination. If either one of the two paths is broken, due to link failure or node failure, one copy of each frame is still able to reach the destination.

1.2 What is PRP

Parallel Redundancy Protocol is another standard (IEC 62439-3 Clause 4) providing redundant Ethernet. Under PRP, each node is connected to two separated, parallel networks (see Figure 24). The nodes send two copies of each frame, one over each network. When a node receives a frame it accepts the first copy and discards the second, eliminating the duplicate frame.

The two networks are assumed to be fail-independent. The destination node will always receive at least one frame as long as one of the two networks is operational. This provides zero-time recovery in case of failure, so no frames are lost.

The downside of PRP is that the network cost is doubled when compared to a single non-redundant network. This makes it more expensive to implement than most of the other redundancy protocols. HSR for example provides the same level of redundancy as PRP, but with lower cost.

1.3 What is Flexibilis Redundant Switch

The Flexibilis Redundant Switch (FRS) is a triple speed (10Mbps/100Mbps/1Gbps) Ethernet Layer-2 switch with HSR and PRP support. FRS is an Intellectual Property (IP) block that can be employed for example with programmable hardware (FPGA). FRS is compatible with IEC 62439-3 Clause 5 ”High-availability Seamless Redundancy (HSR)” and IEC 62439-3 Clause 4 ”Parallel Redundancy Protocol (PRP)”. The Flexibilis Redundant Switch includes also IEEE1588v2 Precision Timing Protocol (PTP) end-to-end transparent clock functionality. IEEE1588 Ordinary/Boundary clock and peer-to-peer transparent clocks are implemented with hardware-software co-operation together with an attached CPU (either hardcore CPU or softcore CPU).

Flexibilis Redundant Switch IP core is available for evaluation purposes free of charge. FRS can be used to implement End-nodes and RedBoxes. (For implementing a Quadbox two FRS cores are needed, but the cores can co-exist at the same FPGA). One of the Ethernet interfaces of the core is typically internal, for the device internal CPU to be able to access the network. Two Ethernet ports are usually used to connect to a redundant network (HSR ring or

PRP LAN). Typically one port is an interlink port that can be used also for maintenance purposes in case of an End-node. Figure 1 shows the typical way to use a 4-port FRS and Figure 2 the CV SoC Configuration.

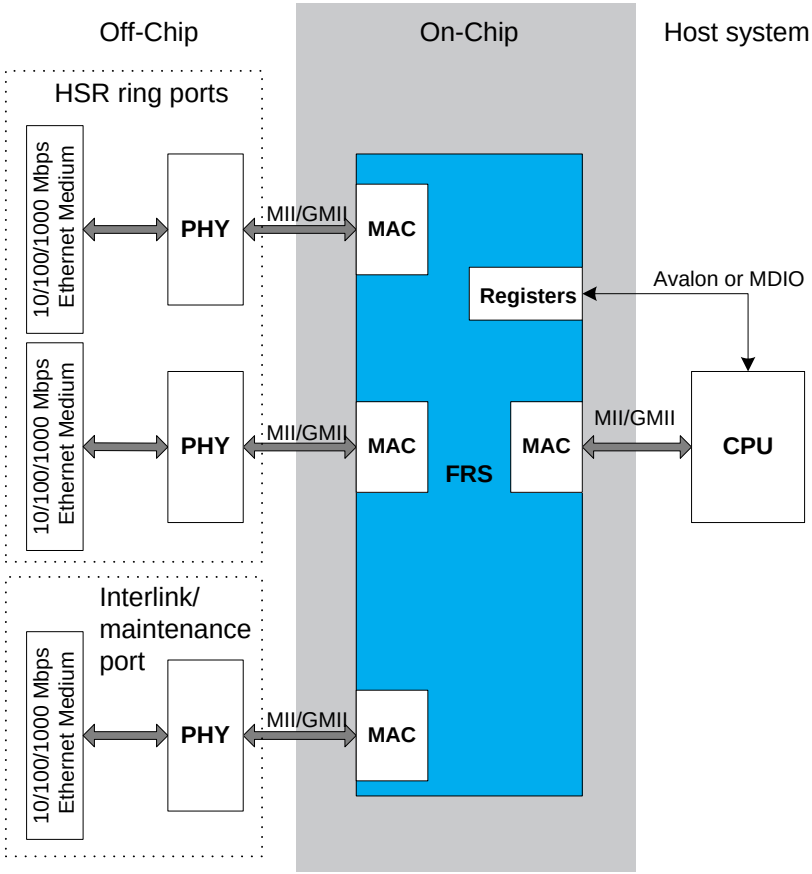

Figure 1. FRS Standard Configuration

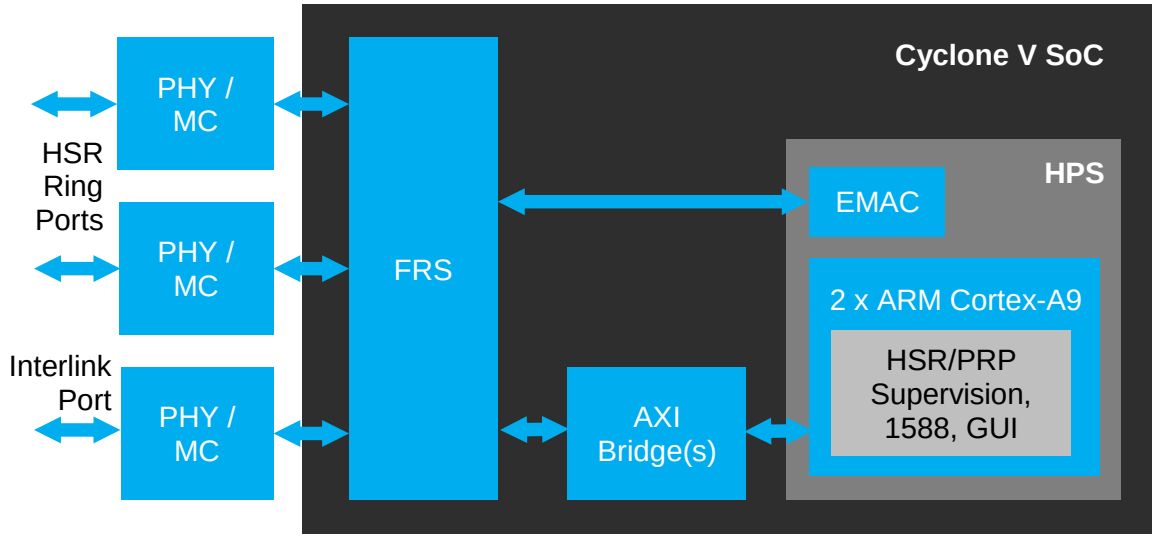

Figure 2. FRS CV SoC Configuration

1.4 About the Test Setup

This document contains instructions on constructing a simple HSR/PRP network setup between two evaluation boards and two Ethernet devices (for example laptops, see Figure 3). This document concentrates on evaluation using Terasic SoC development boards (SoCKit). Terasic SoC development boards can be used for evaluation also together with Altera Cyclone V and Altera Cyclone IV FPGA development boards. In case of such mixed setup, see also http://www.flexibilis.com/downloads/FRS_Demo_CycloneV.pdf and http://www.flexibilis.com/downloads/FRS_Demo_CycloneIV.pdf.

When only two FPGA boards are used, the setup looks exactly the same for HSR and PRP. When there are more than two boards, the setup looks different since HSR network has ring topology and PRP network has double LAN (in this case a double star) topology. Chapters 6 and 7 give more information on how to build a HSR or PRP network between more than two devices. Quadbox setup is presented in Chapter 8.

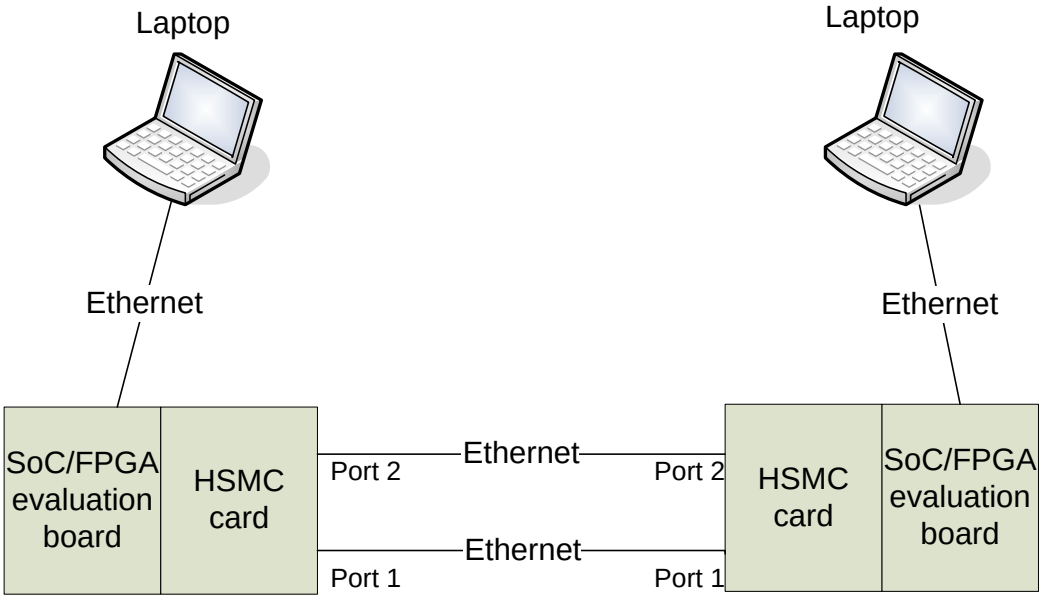

Figure 3. Structure of an Evaluation Setup for HSR and PRP

2 Equipment Needed

The following is the minimum equipment needed for building the evaluation setup (see the next page for information on where they can be ordered from).

- Two Terasic SoCKit Development Kits (optionally the other kit can be replaced by Cyclone V or Cyclone IV FPGA development kit)
- Two Terasic SFP HSMC Boards
- 6 SFP modules. They can be fiber (see Figure 4 and Figure 5) or copper SFP modules (see Figure 6) depending on what kind of cables are used (fiber or copper). Most probably you will need at least two copper modules, to be able to connect to laptops for example.
- Four Ethernet cables (fiber or copper, single or multimode). Most probably at least two of them need to be copper Ethernet cables (for connecting to laptops, test equipment, webcam, etc.). All copper cables should be crossover type.
- Power adapters for the boards (comes with the evaluations boards)
- Two laptops (or other computers, or other test equipment that is able to send/receive Ethernet frames, for example a web camera)
- Six 8mm standoffs and eight 15 mm standoffs (little metal feets the board can stand on) and fourteen metal nuts (0.217"/5.51mm, M3) for the standoffs.
- Two LC-to-LC or RJ45 couplers (optional). If you use these, you will need two more Ethernet cables (fiber if using fiber cables between the boards, copper if using copper cables between the boards).

Figure 4. SFP Module for Multimode Fiber Optic Cable (Black Latch)

Figure 5. SFP Module for Single Mode Fiber Optic Cable (Blue Latch)

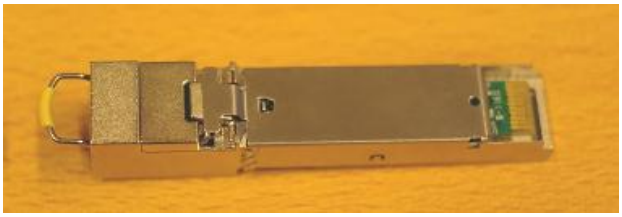

Figure 6. SFP Module for Copper Cable

Note that touching or moving the boards during operation may cause frame loss. This is because of disturbance to the board-to-board signals. You can use LC-to-LC couplers (Figure 7) or RJ45 couplers (Figure 8) between the boards to avoid touching them while connecting

or disconnecting links. If you decide to use these, you will need two more cables (six altogether).

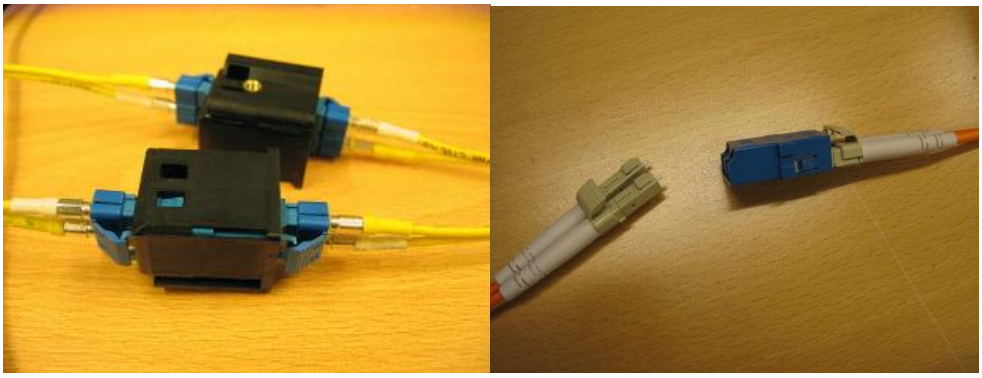

Figure 7. LC-to-LC Couplers (for Fiber Optic Cables)

Figure 8. RJ45 Coupler (for Copper Cables)

The following lists the recommended places from where the equipment needed can be ordered from:

- Terasic SoCKit Development Kit from Terasic: http://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&CategoryNo=167&No=816
- Power adapter for the board is included in the Development Kit.
- Terasic SFP HSMC Board: http://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&CategoryNo=71&No=342
- SFP module for multimode fiber cable from Digi-Key: http://www.digikey.com/product-search/en?x=15&y=12&lang=en&site=us&KeyWords=afbr-5715alz. Typically multimode cables are orange in color and the SFP module latch is black (see Figure 4).
- SFP module for single mode fiber cable from Digi-Key: http://www.digikey.com/product-search/en?x=15&y=12&lang=en&site=us&KeyWords=afct-5715alz. Typically single mode cable is yellow in color and the SFP module latch is blue (see Figure 5).
- SFP module for copper cable from Digi-Key: http://www.digikey.com/product-search/en?x=28&y=20&lang=en&site=us&KeyWords=FCLF-8521-3
- Single mode fiber optic cable from Digi-Key: http://www.digikey.com/product-detail/en/1435791-1/1435791-1-ND/1889887
- Multimode fiber optic cable from Digi-Key: http://www.digikey.com/product-detail/en/9-6374659-7/9-6374659-7-ND/2326175
- Copper crossover cable (RJ45) from Digi-Key: http://www.digikey.com/product-detail/en/219153-1/219153-1-ND/1892833
- LC-to-LC coupler from Digi-Key: http://www.digikey.com/product-detail/en/1828074-3/A99592-ND/1971501

- RJ45 coupler from Digi-Key: http://www.digikey.com/product-detail/en/555051-1/A9108-ND/150720
- 8 mm standoff from Digi-Key: http://www.digikey.com/product-detail/en/R30-3000802/952-1499-ND/2264480
- 15 mm standoff from Digi-Key: http://www.digikey.com/product-detail/en/R30-3001502/952-1506-ND/2264487
- 0.217" (5.51mm) M3 nuts from Digi-Key: http://www.digikey.com/product-detail/en/MHNZ%20003/H762-ND/274973

The whole packet including everything necessary for the evaluation can also be ordered from Flexibilis. Please contact contact@flexibilis.com for further information.

For the Terasic boards you may also contact your local Altera distributors.

3 Software Needed

The software mentioned here should be located on the computer that will be used for creating the microSD (Secure Digital) card for the SoC board. The microSD card will contain all the software and the FPGA program for the SoC board, no separate programming of the SoC board is needed. Insert the SD card that comes with the SoC kit to a SD card reader. Newer laptops typically have an internal SD card reader, and a USB adapter comes also with the SoC kit.

First you'll need to have the Flexibilis Redundant Switch Reference Design packet (FESHASXE04-FBIT.zip) somewhere on the computer; the location of the file doesn't matter. If you don't yet have it, please download it from http://www.flexibilis.com/products/downloads. In addition to the SD card image file itself the packet also contains Release Note and other documentation.

Next you'll need to download and install software that is able to copy the SD card image to the SD card. HDD Raw Copy Tool from HDD Guru is recommended, it can be downloaded at http://hddguru.com/software/HDD-Raw-Copy-Tool/. It needs to be installed with admin rights, otherwise it will not write to the card.

4 Setting up the Evaluation

If you haven't used Terasic boards before, the documentation might be useful as it contains some instructions. It can be downloaded at www.terasic.com.tw/cgi-bin/page/archive_download.pl?Language=English&No=816&FID=a9e8cb474881606fa975d2420a309fb6

See Figure 9 and Figure 10 for two different versions of the simple evaluation setup.

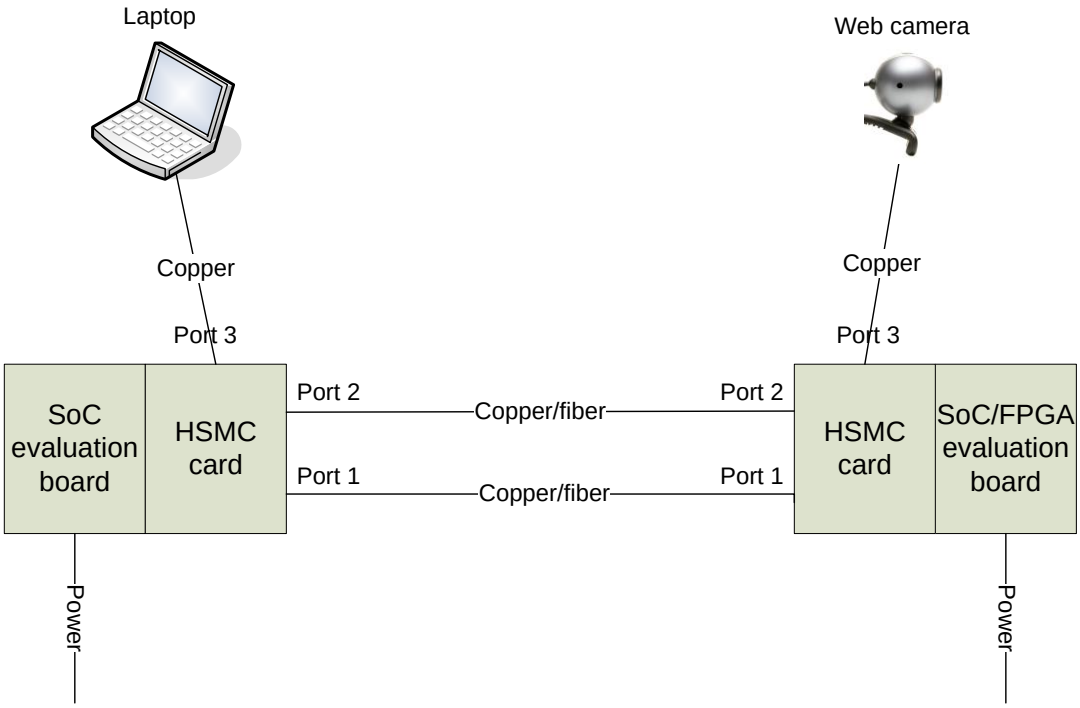

Figure 9. HSR/PRP Setup with Laptop and Web Camera

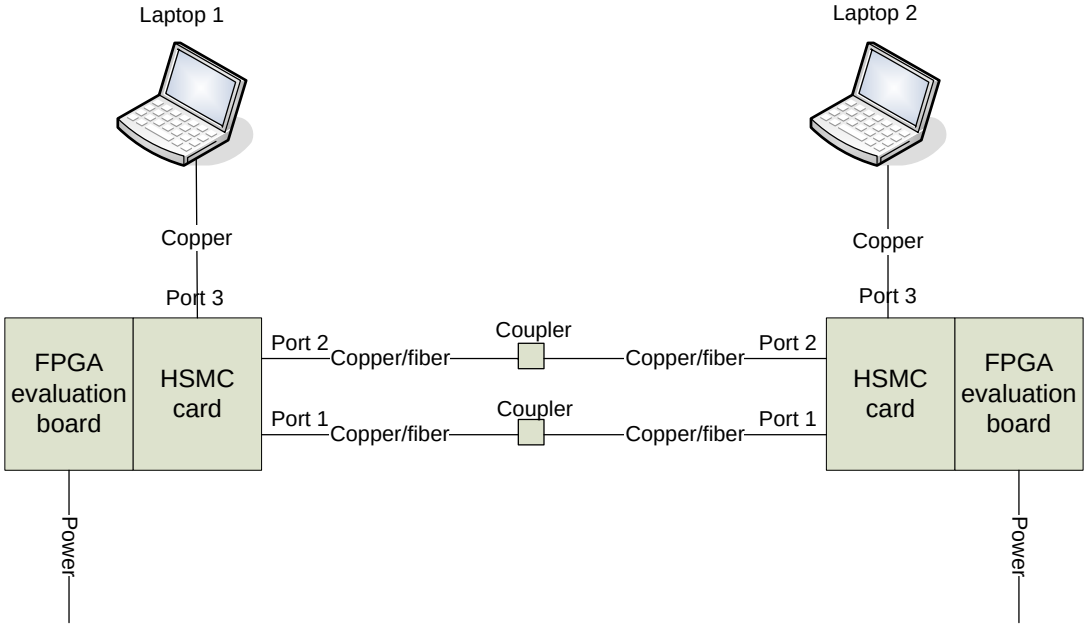

Figure 10. HSR/PRP Setup with two Laptops and Couplers

4.1 Connecting the Boards Together

First you should connect the HSMC boards to the SoC boards. Using standoffs with the boards is recommended but not absolutely necessary (standoffs are the little metal feet the board can stand on). The 15 mm standoffs should go under the HSMC board and the 8 mm standoffs under the SoC board. Use the nuts to tighten the standoffs to the board.

Connect a power cable to the SoC board. See Figure 11 for the setup with SFP HSMC board.

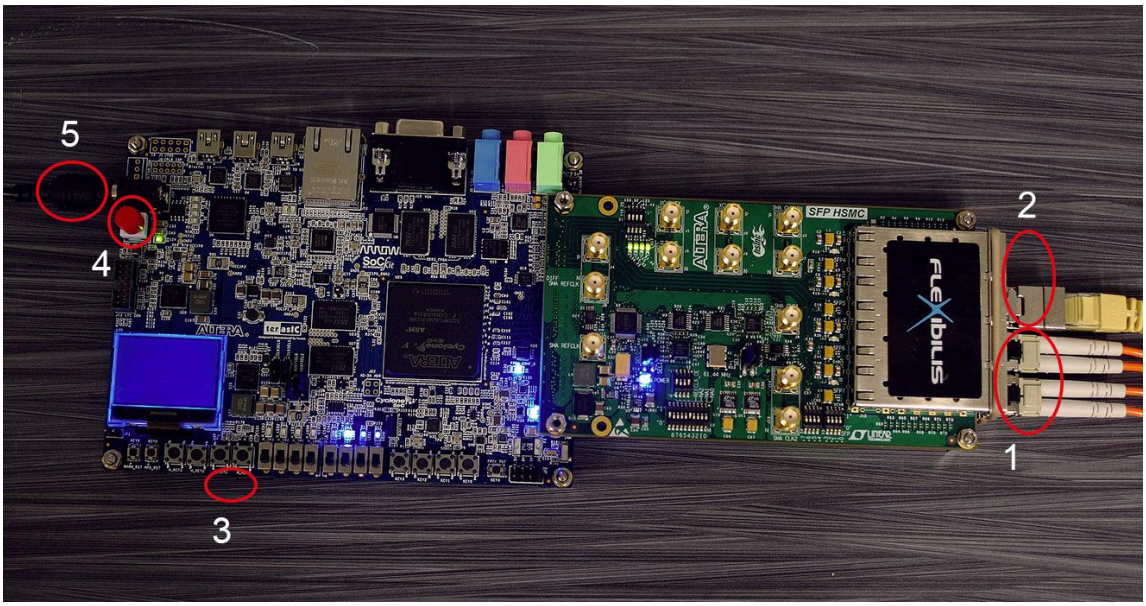

Figure 11. SoC Board Connected to SFP HSMC board

In Figure 11 the red circle 1 is Ethernet ports 1 and 2 for connecting to HSR ring or to PRP LANs. The circle 2 are the interlink ports 3 and 4 going to a laptop/other device used for testing the setup. The red circle 3 is the microSD card reader under the board. Circle 4 is the power switch and circle 5 is the connector for the power cable.

4.2 DIP Switches and Jumpers

In the SoC demo boards the port modes (HSR/PRP) are not configured with DIP switches as in FPGA demo boards. The DIP switches on top of the board can stay in factory settings, as in Figure 12.

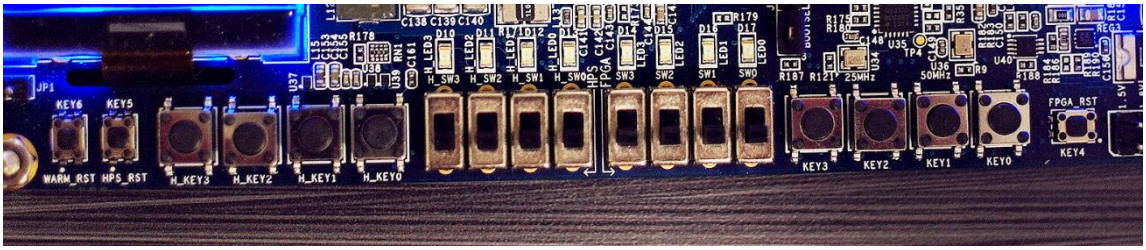

Figure 12. Terasic SoC DIP Switches

The only DIP switch that needs changing from factory settings is SW6 that is at the backside of the board, see Figure 13. It should be as follows:

SW6.1: 0, ON

SW6.2: 1, OFF

SW6.3: 0, ON

SW6.4: 0, ON

SW6.5: 0, ON

SW6.6: 0, ON

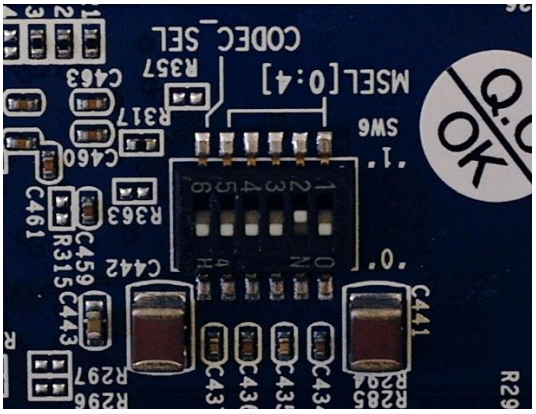

Figure 13. Terasic SoC SW6

The SFP HSMC board DIP switches can be left at their default position, see Figure 14 for reference.

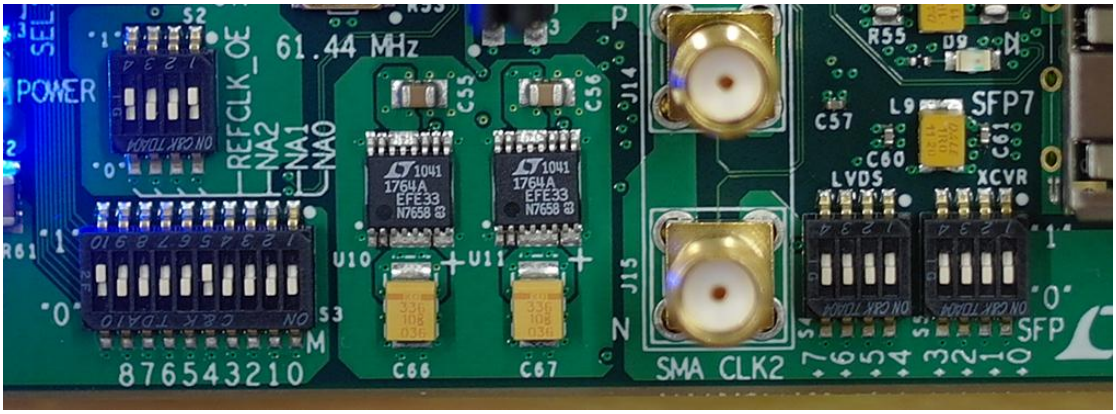

Figure 14. SFP HSMC Board DIP Settings

On the Terasic SoC board, jumpers should be put to the following pins (See Figure 15):

J15: 2-3

J16: 2-3

J17: 2-3

J18: 1-2

J19: 2-3

JP2: 3.3V (7-8)

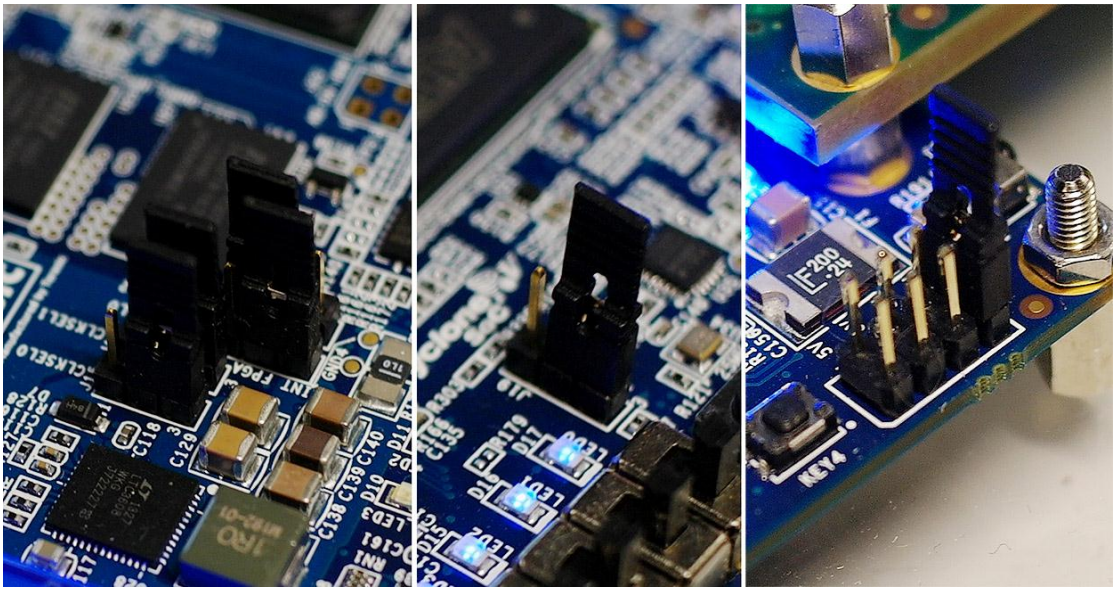

Figure 15. Jumpers on Terasic SoC Board

On the SFP HSMC board, the jumpers should be put to the following pins (See Figure 16):

J12: 1-2

J12: 3-4

J13: 1-2

J13: 3-4

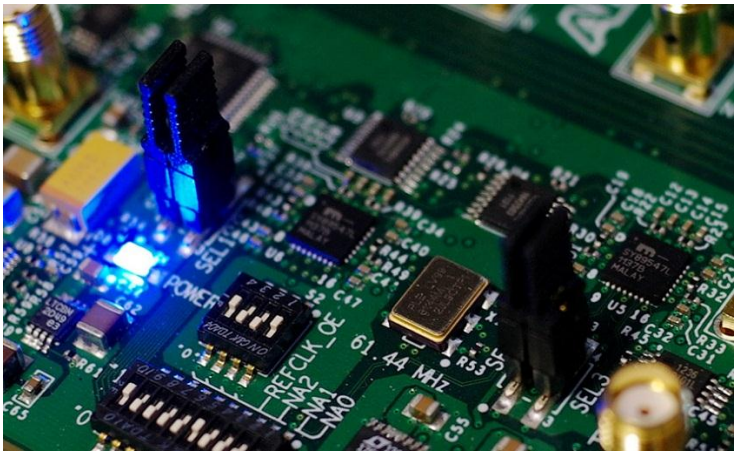

Figure 16. Jumpers on SFP HSMC Board

4.3 Connecting the Cables

Figure 17 shows the SFP HSMC board port numbering.

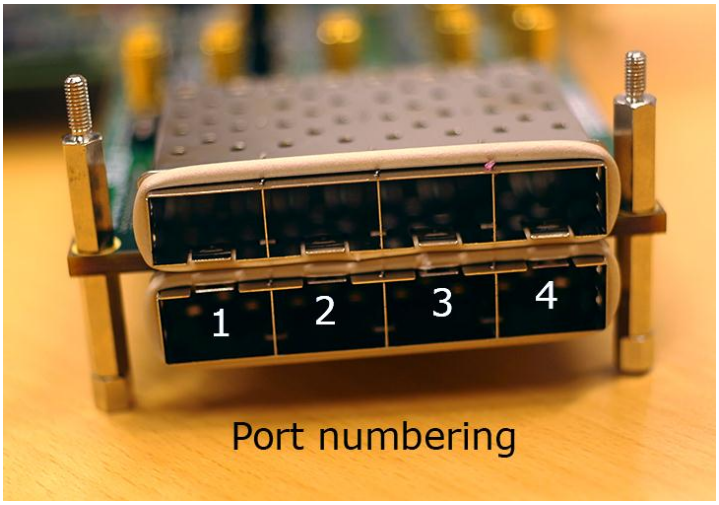

Figure 17. Port Numbering of SFP HSMC Board

Attach an Ethernet cable from the first board port 1 to the second board port 1. To be able to attach the cables to the SFP board you need to use the SFP modules. Also, remember to put the coupler between if you intend to use couplers. Then attach a cable from port 2 to port 2.

Also attach an Ethernet cable from the first laptop to the first HSMC board (port 3) and do the same for the second laptop and the second board. You can replace the laptops with any other Ethernet devices. See Figure 9 and Figure 10 for two alternative versions of the setup.

Please note that every time you disconnect or connect the modules, you need to boot the board, otherwise it will not work. Disconnecting the cable only does not cause this, so for example disconnecting the couplers doesn't require reboot.

4.4 SD Card

Unzip/extract the FRS Reference Design packet (FESHASXE04-FBIT.zip) somewhere on your computer if you haven't done so already. Unzip/extract the SD card image file cyclone5socterasicdevkit/bin/xr7-socfpga-altera.raw.zip.

Use the microSD with SD adapter, and insert the SD card of the SoC board to the SD card reader of the PC. It doesn't need to be formatted. Use HDD Raw Copy tool (Chapter 3) to copy the SD card image (xr7-socfpga-altera.raw) to the SD card. If you are using GNU/Linux, you can use dd command to do the copying.

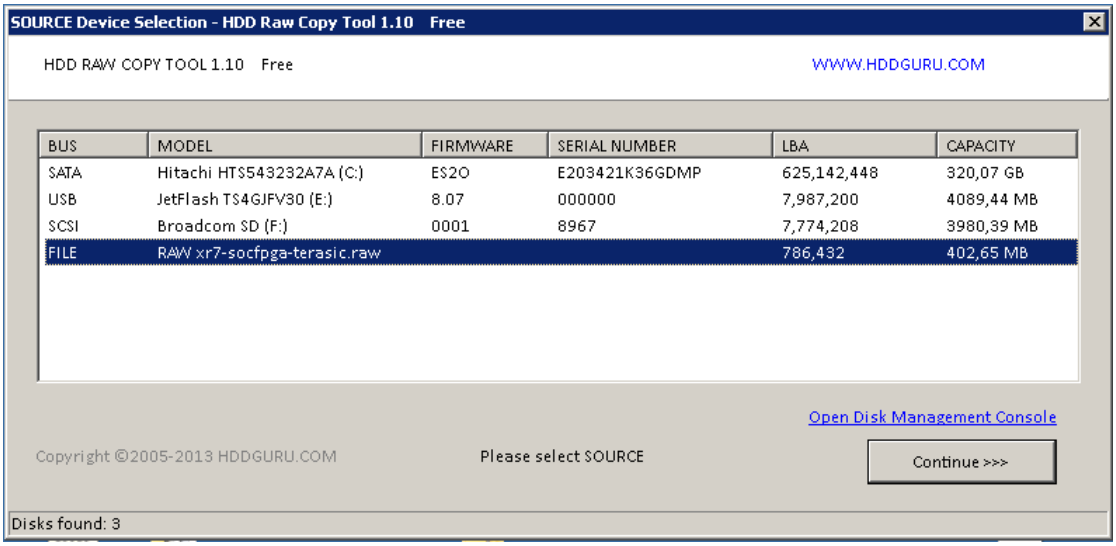

Figure 18. HDD Raw Copy Tool source

Source should be the raw file (Figure 18), and target should be the SD card (Figure 19). Be careful not to accidentally overwrite your other disks.

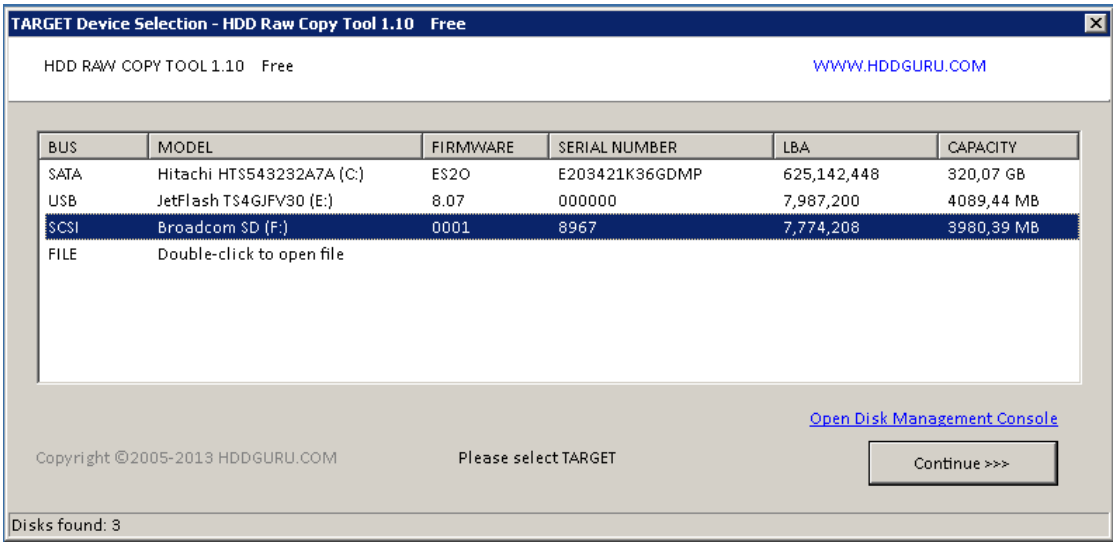

Figure 19. HDD Raw Copy Tool target

Wait for the program to finish. Repeat the procedure for all the SD cards (for all the SoC boards).

Turn off the SoC boards, insert the SD cards, and turn on the SoC boards. Now the software should load itself from the SD card and also program the FPGA.

4.5 Configuring IP Addresses

The laptops or other devices connected to the HSR/PRP network should be in the same IP subnetwork with each other and with the SoC board(s). The default IP address of the SoC board is 192.168.7.1.

To use the HSR/PRP network, a static IP address should be defined for all the devices. In Windows 7, this can be done at **Start** –> **Control Panel** -> **Network and Internet** -> **Network and Sharing Center** -> **Change adapter settings** -> **Local Area Connection** -> **Properties** -> **Internet Protocol Version 4** -> **Use the following IP address**. Administrator rights are needed to be able to change the IP address.

You can change the IP addresses for example to 192.168.7.2 (the first laptop), 192.168.7.3 (the second laptop) and the subnet mask to 255.255.0.0 for both laptops. If you are using some other device, like a web camera, check from its instruction manual how to change its IP address. Alternatively you can check its default IP address from the manual and change the IP addresses of the other devices so that they are all in the same subnetwork. If you have more than one SoC board, connect your laptop first with one SoC board only and change its IP address so that it won't collide with the other SoC board (see Chapter 4.6).

In Windows 7, the current IP address of the computer can be checked at **Start** -> **All Programs** -> **Accessories** -> **Command prompt**. Type **ipconfig** and press enter. This will show you all the IP addresses of the computer. Search for the line that says "Ethernet adapter Local Area Connection" and under that you can see the IPv4 address and subnet mask (see Figure 20).

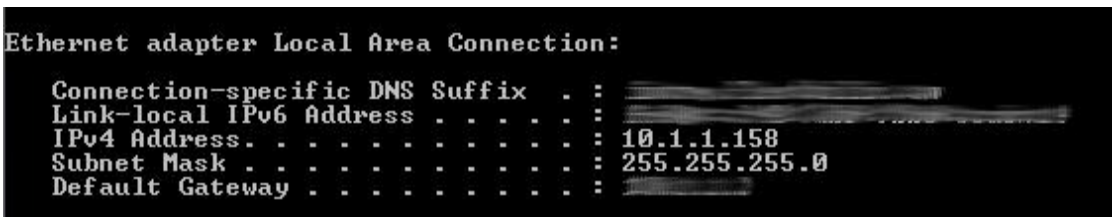

Figure 20. Checking the IPv4 Address

4.6 Graphical User Interface

The Graphical User Interface (GUI) of the SoC board is accessible at address https://192.168.7.1/ . Use the GUI to change the settings of the SoC board. You can for example change the mode of the board between normal Ethernet switch (FES), HSR Redbox, PRP Redbox, HSR-HSR Redbox (half Quadbox) and PRP-HSR Redbox. If you have more than one SoC board in your network use the GUI to change the IP addresses of the SoC boards.

At login screen use “admin” for both username and password and leave IP address field empty. Figure 21 shows the GUI.

Figure 21. SoC Board GUI

5 Testing

5.1 Testing the Connection

At this point your setup is ready to be tested. This can be done by transferring traffic of some sort, for example by FTP if you have FTP server and client installed. Another possibility is to ping from one laptop to another.

In Windows 7, you can ping another computer or other device by first opening the command prompt (**Start** -> **All Programs** -> **Accessories** -> **Command prompt**). Then type **ping** and the IP address you are trying to connect to (for example **ping 192.168.7.3**) and press enter. Figure 22 shows how the response looks like if everything works correctly.

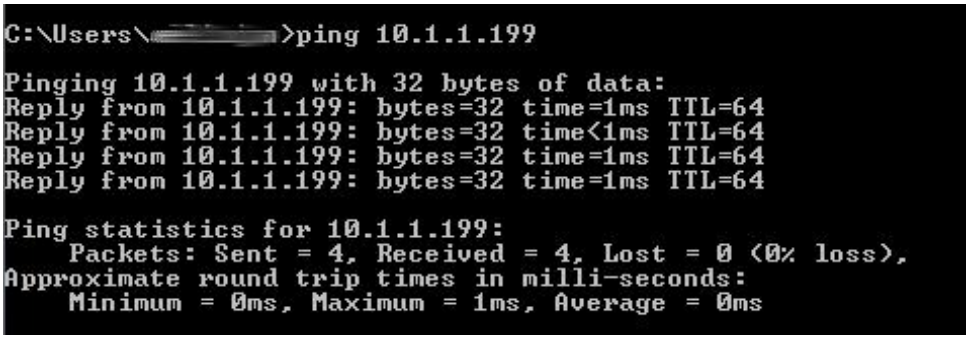

Figure 22. Ping Command

By typing **ping 192.168.7.3 –t** you can ping until **CTRL+C** is pressed. During the file transfer/ping you can disconnect either one of the PRP/HSR links without disturbing the file transfer/ping. Remember to disconnect using the LC or RJ45 couplers. Touching the boards can cause frame loss. Now you can check from the ping output that there was no packet loss.

There is a time limit of **2 hours** for the evaluation. After the time runs out, the boards stop working. If this happens, just turn off the boards and then turn them on again. This will reset the FPGA and it starts counting the evaluation period from the beginning.

5.2 LCD Display

The FRS doesn't have a LCD display menu system for SoC board. That is replaced by the Graphical User Interface (GUI) presented in Chapter 4.6.

6 HSR with Three or More Boards

HSR is typically used with ring topology. Any link in the ring can be disconnected during the operation without interrupting the traffic. A board can be turned off without interrupting the traffic of other nodes in the ring. For example in Figure 23 the board that has no laptop connected can be turned off without interrupting the traffic between the laptops.

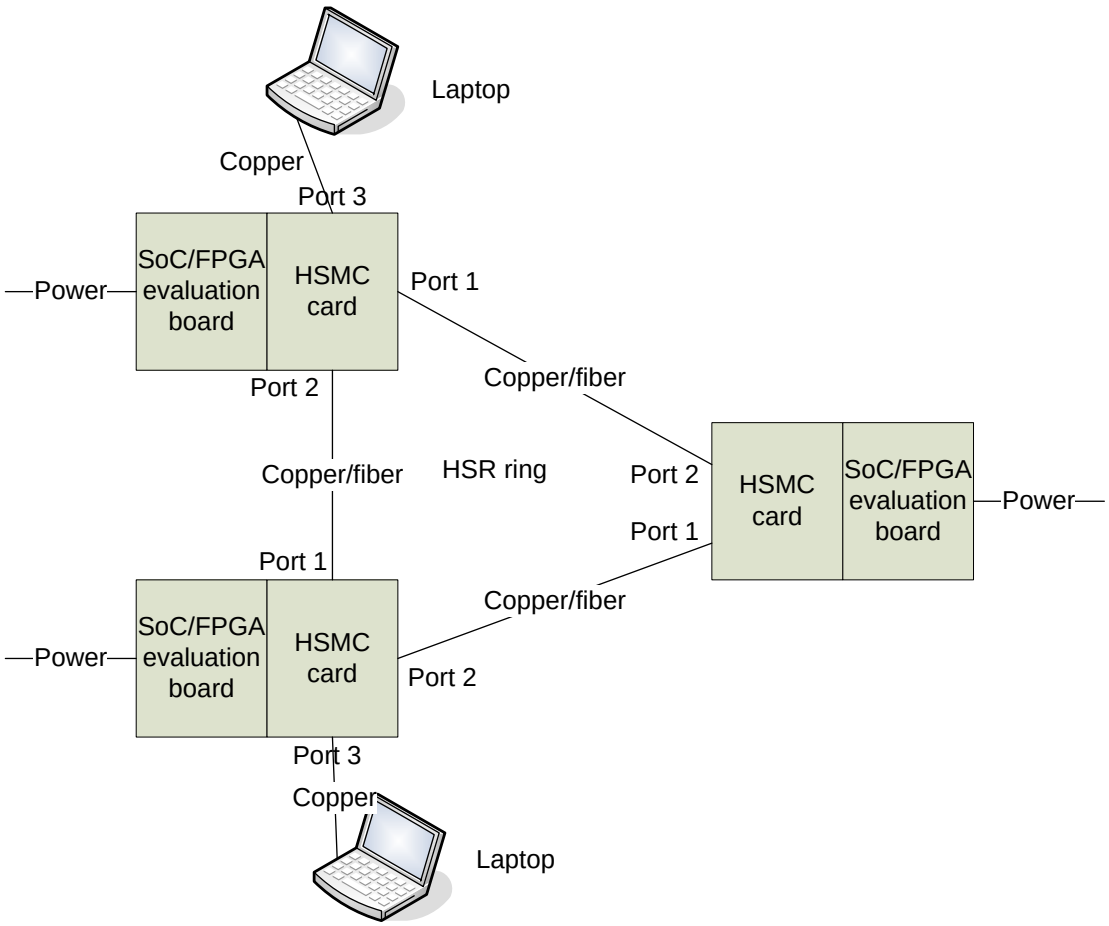

Figure 23. HSR Ring between Two Laptops

Note that the HSR ring consists of links connected to ports 1 and 2. The test devices (for example laptops) can be connected to port 3 or to port 4.

7 PRP with Three or More Boards and with Ethernet Switches

PRP is typically used with double LAN topology (not a ring). Normal (non-PRP-aware) Ethernet switches can be used in LAN_A and LAN_B. Any link can be disconnected during the operation without interrupting the traffic. Also, either one of the Ethernet switches can be turned off without interrupting the traffic. See Figure 24 for reference.

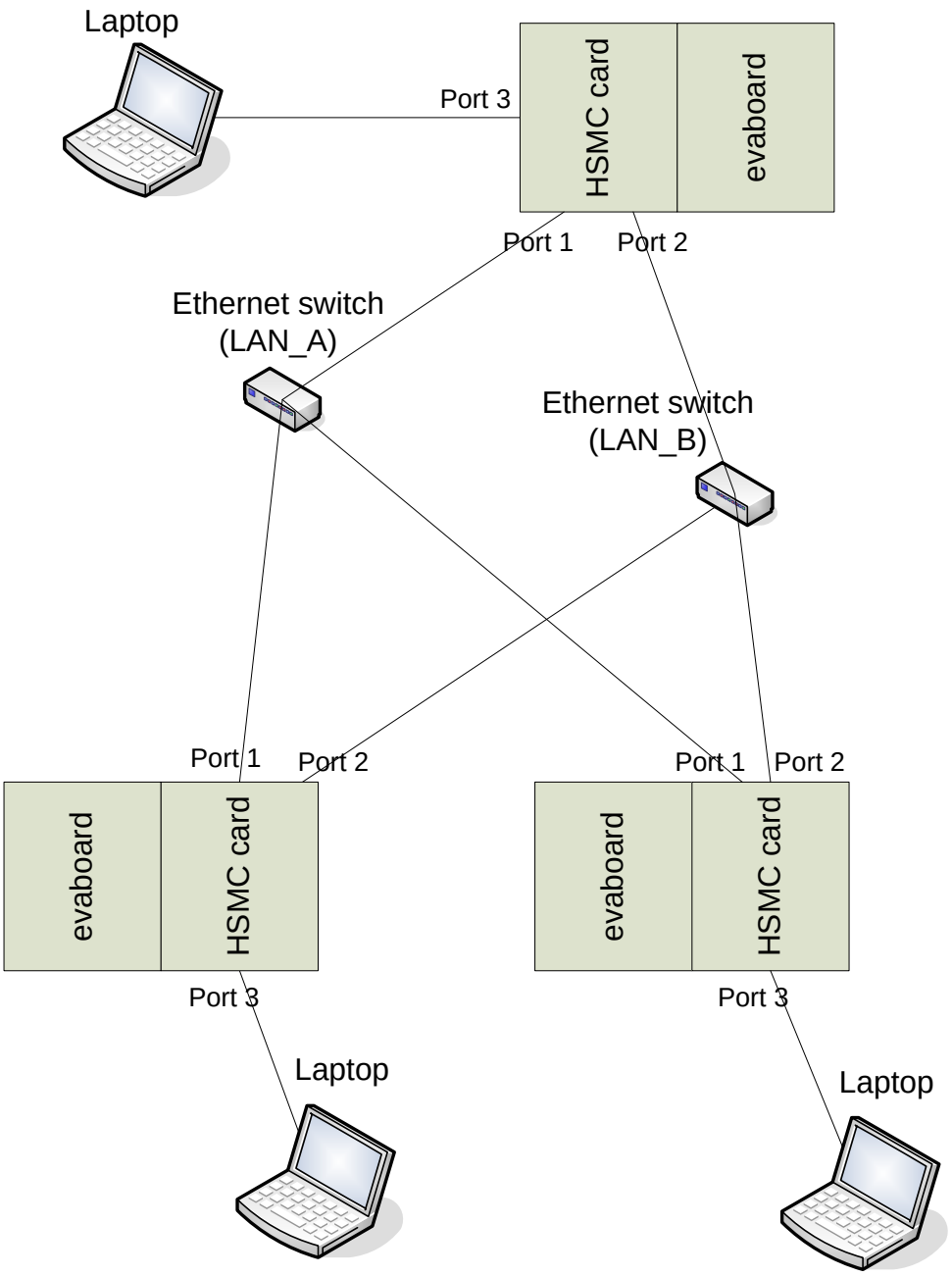

Figure 24. PRP Setup with Three Boards

8 Quadbox Test Setup

A Quadbox connects a HSR ring to another HSR ring. Typically two Quadboxes are used between rings, to remove the single point of failure only one Quadbox would cause. A Quadbox can be constructed using two FRS IP cores. In the end product the two FRS cores can be located on the same FPGA chip. In this demo two Altera boards (one FRS core on each board) are used to form a Quadbox, as presented in Figure 25. The boards acting as half-Quadboxes are configured as HSR-HSR RedBoxes. This means that their interlink port that connects to the other half-Quadbox is in HSR mode.

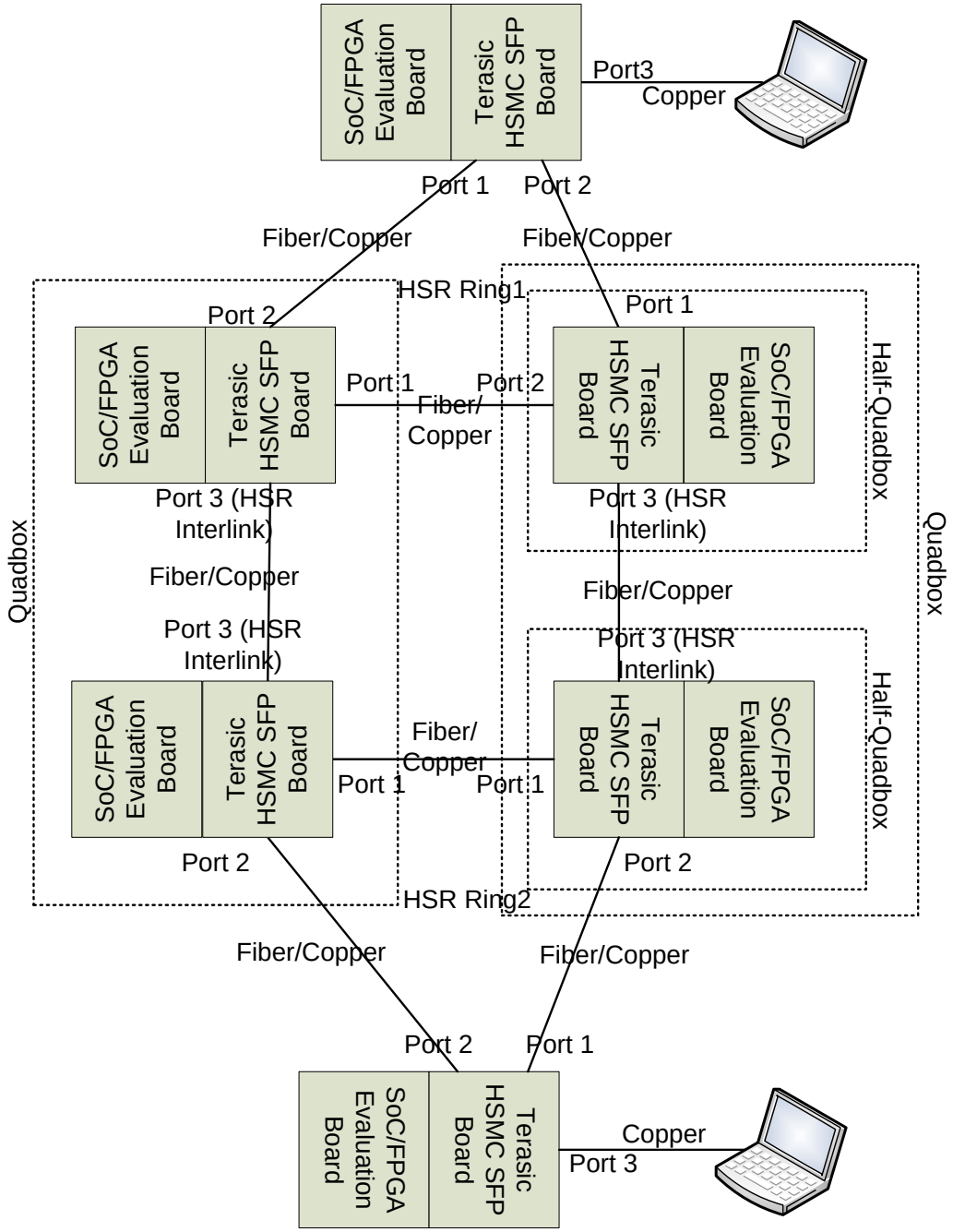

Figure 25. Quadbox Test Setup

9 Troubleshooting

9.1 Link Does Not Go Up

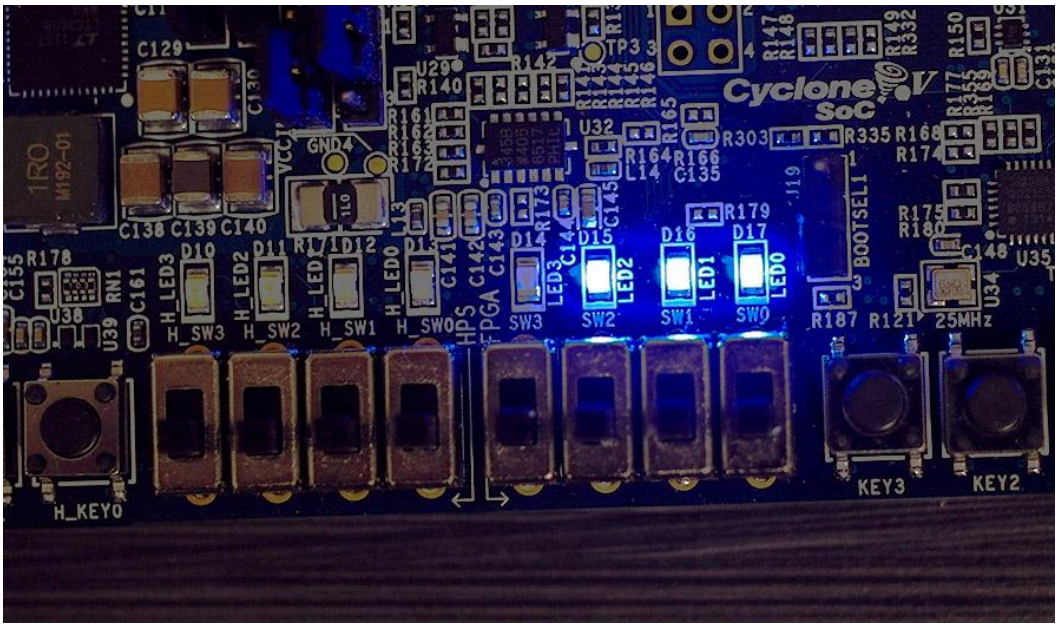

Figure 26. Location of the Link LEDs

Figure 26 shows the location of the LEDs that indicate if the link is up or not. The link LEDs are:

D17: Port 1 (refer to Figure 17)
D16: Port 2 (refer to Figure 17)
D15: Port 3 (refer to Figure 17)
D14: Port 4 (refer to Figure 17)

Also computers and other Ethernet devices typically have link LEDs. The LEDs are usually located next to the Ethernet port and they should be on when the link is up.

If the link LED is not on even though it should be:

- Check that all the cables and SFP modules are properly attached and that the boards are switched on
- Restart the boards (power off, power on)
- Check that fiber optic modules and cables are of the same type
    - Single mode fiber is typically yellow and it should be used only with single mode modules who typically have blue latches, see Figure 5
    - Multimode fiber is typically orange in color and it should be used only with multimode modules who typically have black latches, see Figure 4
- Try changing the cables
- If you disconnected/connected again the SFP modules, you need to restart the board for the network to work again.
- The copper cable has to be the crossover type, so check the cable type. Crossover cable (see Figure 27) has different pinouts at each end, which means that the colored lines (wires) you can see through the plastic at the end of the cable (green, blue, red) are in different order at different ends of the cable. On the other hand, straight cables have the same pinout on both ends. You can see this in Figure 28: on both ends the colored lines at the end of the cable are in order green – blue – red.

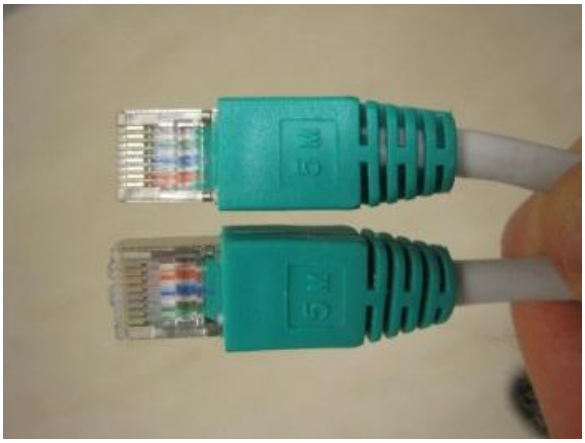

Figure 27. Crossover Cable

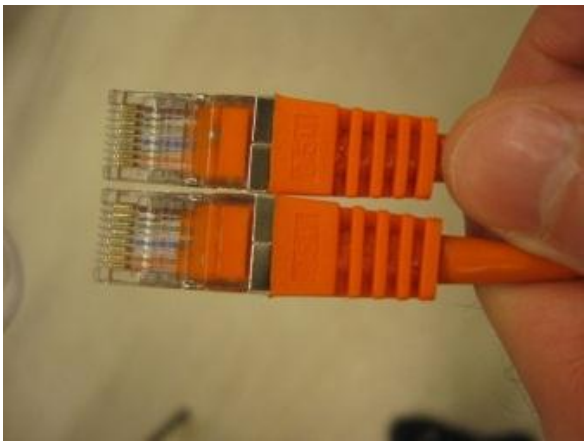

Figure 28. Straight Cable

9.2 File Transfer/Ping Does Not Work

- Check that all the links are up!
- Check the IP addresses: are the computers in the same subnetwork or is there something else wrong with the addresses? See section 4.5 Configuring IP Addresses for how to define the IP addresses.
- Check that file transfer/ping works with a straight connection between the laptops (connect the two laptops to each other with a crossover copper cable)
- Check the firewall settings of the laptops. Try disabling the firewall and see if file transfer/ping starts working.
- There is a time limit of 2 hours for the evaluation. If this time runs out the network will stop working. To get it to work again, turn off the boards and then turn them on again.

10 Appendix 1 Reference Design

A reference design for Altera Cyclone V SoC Development board is provided to make it easier for customers to start making their own FPGA designs around FRS. The reference design can be downloaded from our website.

With the reference design, you can test the functionality of FRS in your own application. This includes testing of IEEE1588 / PTP (Precision Time Protocol) and HSR/PRP. Basically the reference design functions as a HSR/PRP RedBox, which means you can test RedBox functionality with two redundant ports and interlink port(s). The reference design includes everything that is needed around FRS to test its functionality. No licenses are required to test the reference design.

For usage in end products Flexibilis grants Licenses for the Reference Design for free as long as it is used together with Flexibilis FRS product. You can alter the reference design to fit your purposes and environment. The reference design can be compiled with Altera Quartus II tool and the resulting FPGA design can be loaded for example onto Altera Cyclone V SoC Development board. Instructions on how to use the Reference design can be found in this appendix. When compiling for your end product, you might need some licenses, see section 10.7.

10.1 Installing

Unzip the release packet containing the reference design (FESHASXE04-FBIT.zip) to a directory on your computer. To be able to compile the design, you will also need to download the IP cores, see section 10.6.

10.2 Using with Quartus

Install correct version (see release note) of Quartus II software and open the Quartus II project in Quartus II by double clicking the file soc_system.qpf. The top level of the design is in the file named fpga.vhd. Before the whole design can be compiled, QSYS generate has to be run first: Start by selecting Tools -> Qsys from the drop-down menu. Open soc_system.qsys. Compile by pressing Generate button at the generate page. Compiling the whole design can then be done by selecting Processing -> Start Compilation in the Quartus II drop-down menu.

10.3 Block Diagram

The structure of the design can be viewed with QSYS tool. The structure of the reference design is presented in Figure 29.

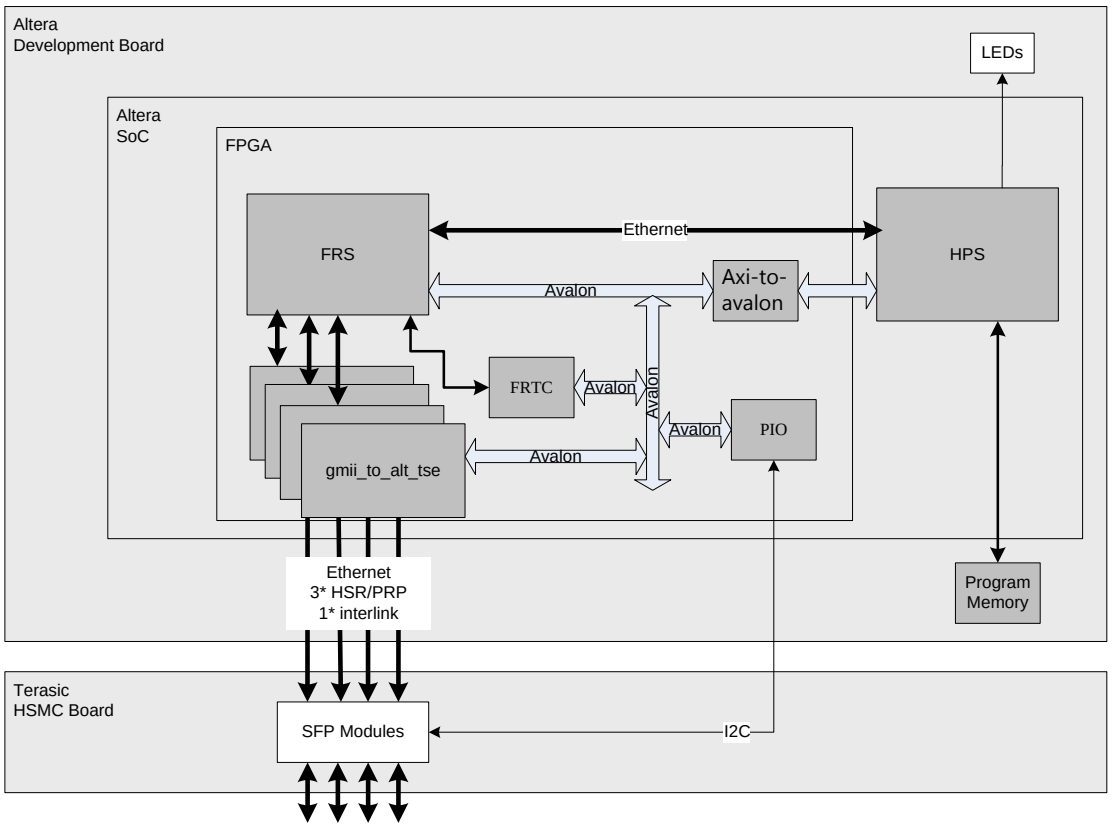

Figure 29. Reference Design Block Diagram

10.4 Main Blocks

The main blocks of the FPGA reference design are FRS, FRTC and gmii_to_alt_tse. These are presented in the following subparagraphs.

10.4.1 FRS (fes)

Flexibilis Redundant Switch with HSR and PRP Support, formerly known as “FES-HSR”. This block is encrypted so that the vhdl code cannot be viewed. It has 2 hour evaluation limit, after which the design stops working. FPGA reboot/reload is needed to restart the evaluation period. See FRS Manual for more information on FRS.

10.4.2 FRTC

Flexibilis Real-Time Clock (FRTC) provides adjustable wall clock time for FRS.The clock time is used for IEEE 1588v2 transparent clock and frame timestamper functionality of FRS.

10.4.3 gmii_to_alt_tse

The gmii_to_alt_tse block alters the GMII interface of FRS to a 1000BASE-X interface compatible with SFP modules and 1000BASE-X fiber Ethernet standard when using fiber SFP modules. When copper SFP modules are used, the gmii_to_alt_tse block alters the GMII interface to SGMII.

10.5 How to Modify the Design

Users can modify the reference design, as far as it is used together with FRS. The modifying can be done with QSYS tool and the editor integrated in the Quartus II tool. The modified design can then be compiled and loaded onto Altera Cyclone V SoC Development board or onto some other board (requires modification of the design if the I/Os and the FPGA model are not the same).

10.6 How to Compile and Download the Compiled Design to the Board

To be able to compile the design, the FRTC and FRS IP cores are needed. The FRS IP core can be downloaded from https://www.altera.com/solutions/industry/industrial/applications/smart-energy/ind-smart-grid.html. Click “Request IP”. To download it, you will need to enter the part number/product code FESHA00E00-FBB.

Create a directory named *encrypted_ip* on the main level of the reference design directory (first level, in the same directory with *cyclone5socdevkit* and *doc*).

Unzip the IP core packet downloaded from the Altera site. There you can find a directory named *core*. Copy the contents of this directory to the *encrypted_ip* directory you created before.

The FRTC IP can be downloaded from Flexibilis webpage: http://www.flexibilis.com/products/downloads/. Create a directory named *external* under *cyclone5socdevkit* directory and *frtc* directory under external. Then copy files from frtc IP release *core* directory to *external/frtc/*.

Now you should be able to compile the design. If the compilation doesn’t succeed, try reconfiguring the license files. In Quartus II, this can be done at **Tools -> License Setup**.

Depending on the type of changes made to FPGA design, Preloader may have to be rebuilt and reinstalled too. Information on how to do this can be found from FRS_SoC_evaluation_design.pdf (comes with the reference design zip packet), chapter 4.4.2. Also chapter 4.1.2 has information about the Preloader.

The design is compiled by selecting **Processing -> Start Compilation** from the Quartus II drop-down menu. A successful compilation will result a file named fpga/bin_qsys/output_files/soc_system.sof.

The soc_system.sof can then be converted into .rbf form by running “quartus_cpf.exe -c -o bitstream_compression=on output_files/soc_system.sof output_files/soc_system.rbf”

Copy the soc_system.rbf file to the /boot directory on the SD card (the first partition, note ext2 filesystem) and the FPGA will be programmed with it in the bootup.

10.7 The Licenses Needed and How to Get them

Depending on your design, there are certain licensable products that might be needed in your design. Testing with the reference design on Altera V SoC development boards doesn’t require any licenses. However, when you have your own devices ready and you are compiling the binary for production, all the licenses need to be in check.

TSE, Triple-Speed Ethernet IP (Altera)

TSE is needed only if SGMII/1000Base-x interfaces are used. TSE is also available as an Open Core Plus (OCP) license that makes evaluation possible. With the OCP license the IP works for one hour.

Linux Application Software (Flexibilis)

Please contact Flexibilis.