Reliable Ethernet

Flexibilis Redundant Switch (FRS)

Flexibilis Redundant Switch (FRS) is an IP core providing HSR/PRP functionality. Thanks to its scalability, the single IP core can be easily used both in low as well as high-end devices based on FPGA technology.

FRS has been validated using sophisticated methods that quarantee the quality of the IP – for example HW accelerated simulation. The ready-made reference systems enable rapid and predictable product development cycle while still benefiting from the flexibility of FPGA technology.

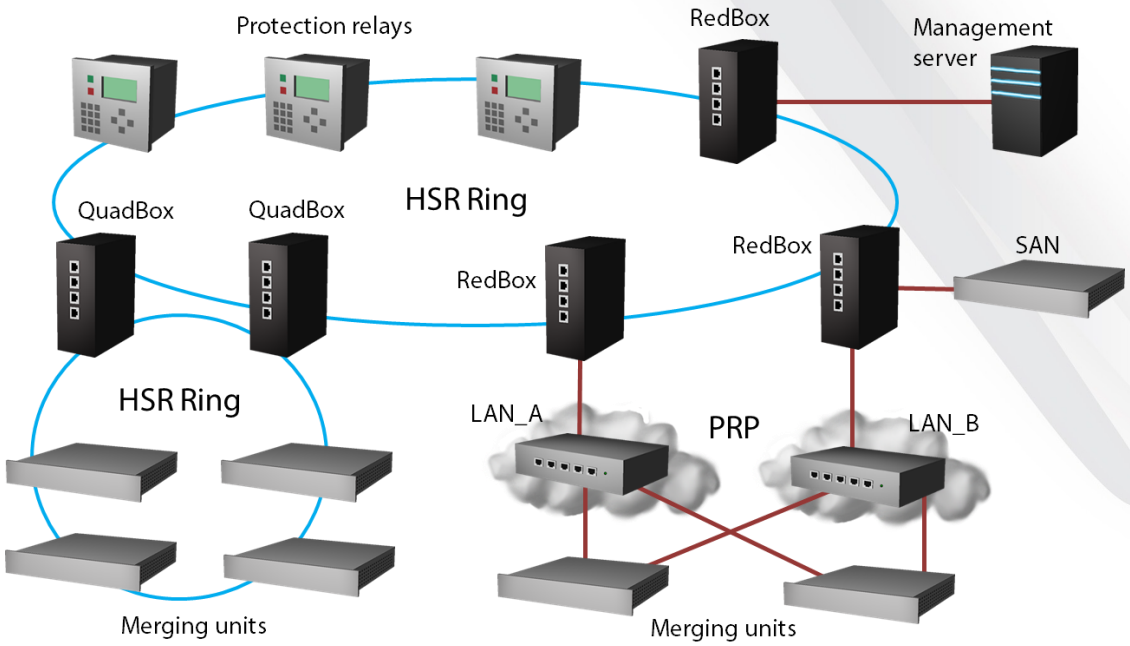
To support HSR protocol in a device at least three port HSR switch is needed: two ports for HSR and one interlink port e.g. CPU. However, additional Ethernet ports are needed in many cases, for example in RedBoxes. FRS is compatible with Altera FPGAs.

High-availability Seamless Redundancy and Parallel Redundancy Protocol

HSR and PRP protocols are used in applications that require short reaction time and high availability. They provide a network that has no single point of failure and zero recovery time in case of a failure: Single network faults will not result in any frame loss. The network is fully operational even during maintenance as any network device can be disconnected and replaced without breaking the network connectivity.

Applications for HSR/PRP

- Substation automation
- Industrial automation
- Vehicle communication
- Network equipment



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Feature	Benefit
From three to eight triple-speed 10/100/1000 Mbit/s ports, full-duplex on all ports	The scalability makes it possible to use the same IP Core in both low as well as high-end devices. Gigabit speed means also less latency.
HSR (High-availability Seamless Redundancy) -HSR RedBox, HSR End node and HSR QuadBox support	Cost-efficient and standardized redundancy method with zero recovery time.
PRP (Parallel Redundancy Protocol) -PRP RedBox and DANP support	FRS is compatible also with PRP devices.
RSTP support	Network loop detection and removal.
GbE switch -Compatible with IEEE standard 802.1D Media Access Control (MAC) Bridges	Traditional Ethernet switch functionality included.
Packet forwarding at wire-speed, non-blocking	The switch core can handle the maximum amount of traffic defined by the Gigabit Ethernet standard, all ports at the same time.
PTP (Precision time Protocol) -End-to-end one-step Transparent Clock -Peer-to-Peer Transparent Clock support -Ordinary/Boundary Clock support	No need for separate time synchronization network, for example IRIG-B. Instead the time information can be shared through the HSR/PRP network. Nanosecond class accuracy in clock synchronization can be reached.
Interface options: MII and GMII (RMII, RGMII, SGMII, 1000BASE-X and 100BASE-FX with optional adapters)	Supports the most used interfaces for connecting to physical layer devices (PHYs) and microcontrollers, as well as the Gigabit and 100Mbit standards for connecting directly to optical transformers.
Avalon and MDIO interfaces	Standardized methods for accessing control and status registers.
Cut-through and Store-and-Forward operation	Preferred forwarding method can be chosen: Cut-through mode minimizes latency while Store-and-Forward offers greater reliability.
Quality of Services (QoS) with priority tagging, packet filtering and four priority queues per port	Important packets can be prioritized which minimizes latency of higher priority traffic.
Port-based VLAN and VLAN tagging -Max number of VLANs is 4096	The network can be segmented which can simplify network design and management.
Support for MAC address based authenticating methods	Security by authenticating connected devices.
RMON statistics counters	SNMP support for network monitoring purposes.

Flexibilis and Altera offer a royalty based business model for licensing FRS with no per-unit royalty reporting, no upfront licensing fees and no license negotiations. When going into production, all that is needed is a security chip that can be purchased from Altera.

- Reduce development risk
- Faster time to market
- Evaluate for free for an unlimited time period

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