PRODUCTS AND LICENSING

Revision History

Rev	Date	Comments
1.0	18.09.2014	First version
2.0	14.06.2016	Product assortment updated
2.1	2.12.2016	XRS Family product line added
2.2	21.4.2017	Product assortment updated
2.3	16.8.2019	Document updated

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1 About This Document

This document gives an overview of the products that Flexibilis provides. Based on this document, the customer should be able to notice other products that would add value on their end-product but also understand which products may be needed to generate designs.

Chapter 2 describes XRS product family, Chapter 3 introduces the main FPGA IP Cores and Chapter 4 XR7 Software. Chapter 5 defines the available Reference Designs and Chapter 6 introduces shortly services related to Flexibilis products. Chapter 7 shows a product matrix for a couple of use cases and Chapters 8 and 9 define Abbreviations and References.

2 XRS Product Family

This chapter describes all products related to XRS Family.

2.1 SpeedChips XRS Devices

XRS switches are integrated semiconductor devices for adding HSR, PRP and time synchronization functionality to existing and new applications. XRS switches are part of Arrow Electronics' SpeedChips product family.

2.1.1 XRS7000 Series

There are two different XRS7000 versions available: XRS7003 (three ports) and XRS7004 (four ports). XRS7003 can be employed in HSR and PRP end nodes and XRS7004 in both end nodes and HSR and PRP RedBoxes. A QuadBox can be built using two XRS7004 devices.

Features:

- Compatible with High-availability Seamless Redundancy (HSR)
- Compatible with Parallel Redundancy Protocol (PRP)
- Two (XRS7003) or three (XRS7004) 10/100/1000 Mbit/s RGMII ports
- Time and frequency synchronization using IEEE1588-2008 Precision Time Protocol v2
- I^2C and MDIO for register access
- Cut-through and store-and-forward operation
- Quality of Services (QoS) with priority tagging, packet filtering and four priority queues per port
- Port-based VLAN and VLAN tagging
- PPS (Pulse per Second) input and output
- Support for MAC address based authenticating methods
- RMON statistics counters
- Two industrial range packages available: 144-Pin Plastic Enhanced Quad Flat Pack (EQFP) and 256-Pin Fine Line Ball Grid Array (FBGA)

All the chips are available from the Arrow webshop with the following product codes:

ARWSC-XRS7003E (three ports, 144 EQFP package): https://www.arrow.com/en/products/arwsc-xrs7003e/arrow-development-tools

ARWSC-XRS7003F (three ports, 256 FBGA package): https://www.arrow.com/en/products/arwsc-xrs7003f/arrow-development-tools

ARWSC-XRS7004E (four ports, 144 EQFP package): https://www.arrow.com/en/products/arwsc-xrs7004e/arrow-development-tools

ARWSC-XRS7004F (four ports, 256 FBGA package): https://www.arrow.com/en/products/arwsc-xrs7004f/arrow-development-tools

2.2 XRS7004E Reference Board

XRS7004E Reference Board can be used for evaluating the functionality of XRS7000 series devices.

Board features:

- XRS7004E Ethernet switch chip
- Three 10/100/1000 Mbit/s Full-Duplex Twisted pair copper Ethernet interfaces with RJ45 connectors
- Three SFP cages for fiber optic Ethernet modules (100/1000 Mbit/s)
- 10/100 Mbit/s CPU port with RJ45 connector
- I^2C and MDIO interfaces for accessing XRS7000 registers
- PPS (Pulse per Second) input and output for time synchronization
- 5 V input power
- Designed to be compatible with Raspberry Pi single-board computer. (SW package for Pi available)

The Board is available from the Arrow webshop with the following product code:

ARWSCBRD-XRS7004E, https://www.arrow.com/en/products/arwscbrd-xrs7004e/arrow-development-tools

2.3 XRS Software

Software that can be used with XRS Devices and/or Reference Boards.

2.3.1 XRS RPi Disk Image

XRS RPi Disk Image is an SD card image for Raspberry Pi which is used with XRS7004E Reference Board. It contains reference software for the board, and is meant for testing and demonstrating the functionality of XRS7000 devices. The prebuilt SD card image allows XRS device evaluation without having to setup the environment and build any software. The software or parts of it can also be licensed for customers employing XRS7000 series devices in their products.

The main parts of the software stack are:

- XR7 PTP for time synchronization
- XR7 Redundancy Supervision for HSR/PRP supervision protocol
- XR7 Management Software for configuration management and status monitoring
- System programs and utilities from Debian GNU/Linux distribution
- Linux kernel
- Linux device drivers

XRS RPi Disk Image can be downloaded from the Flexibilis website:
https://www.flexibilis.com/products/downloads/

2.3.2 XRS Software Environment

The XRS Software Environment contains all necessary tools pre-installed for building and managing software and SD card images for RPi. Build processes are highly automated so that new and custom images can be built with minimum effort. An included build environment provides a cross-compile tool chain for Raspberry Pi, used to build binary packages for the resulting SD card images. The environment is used either with a continuous integration server or with command line via SSH. The environment does not provide a graphical desktop environment.

The delivery package contains:

- Virtual machine disk image including the XRS Software Environment
- XRS RPi Disk Image: Prebuilt Raspberry Pi SD card image for XRS usage
- Release note document
- XRS Reference Software User Guide document

The XRS Software Environment can be downloaded by filling in the form on this page:
https://www.flexibilis.com/products/downloads

3 FPGA IP Cores

This chapter discusses Flexibilis IP blocks for FPGA designs and their licensing methods.

3.1 Flexibilis Ethernet Switch (FES)

The Flexibilis Ethernet Switch (FES) is an Ethernet switch IP block designed to be used in programmable environments. FES includes multiple Ethernet Media Access Controller (MAC) functional entities and provides MII/GMII interfaces for Ethernet PHY devices and optionally for a host system CPU. FES standard features include:

- 10/100/1000 Mbit/s Full-Duplex Ethernet interfaces
- Compatible with IEEE standard 802.1D MAC Bridges
- Media Independent Interfaces (MII) and Gigabit Media Independent Interfaces (GMII) for attaching to external Physical Layer devices (PHY) and host system CPU(s)
- Avalon slave interface for register access
- Ethernet packet forwarding at wire-speed, non-blocking
- PTPv2 end-to-end one-step transparent clock processing at hardware
- PTPv2 peer-to-peer transparent clock support functions
- PTPv2 boundary and ordinary clock support functions
- Ethernet packet filter and prioritization on each of the ports

Additional features that can be licensed on top of standard features include:

- Compatible with IEC 62439-3 ”High-availability Seamless Redundancy (HSR)”
- Compatible with IEC 62439-3 ”Parallel Redundancy Protocol (PRP)”
- Static MAC table
- Traffic policing and shaping
- MACsec

FES with redundant networking features is called Flexibilis Redundant Switch (FRS).

FES with standard features or FRS (FES + HSR/PRP) is provided with the following licensing methods:

- **Open Core Plus black-box** design for evaluation
  - About 2 hours run-time limit
  - For Intel Cyclone IV, Cyclone V and Cyclone V SoC
  - Evaluation version can be requested trough Flexibilis website: https://www.flexibilis.com/frs-ip-core-download/
- **Paid-up license** for production
  - No time limits
  - For Intel Cyclone IV, Cyclone V and Cyclone V SoC. For other device families contact Flexibilis for more information
  - For other FPGAs contact Flexibilis for more information
  - For price and licensing information contact Flexibilis
- For **other licensing methods** please contact Flexibilis

Extra features can be licensed on top of FES or FRS with **paid-up license**.

3.2 FRTC

The Flexibilis Real-Time Clock IP provides a real-time clock, which supports clock adjustment and provides the clock information via registers and external interface. In Addition, the FRTC supports Pulse Per Second (PPS) output signal for external synchronization.

FRTC IP is provided with the following licensing methods:

- **Open Core Plus black-box** design for evaluation
  - Intel FPGA: No device family dependencies
  - Available from http://www.flexibilis.com/products/downloads/
- **Paid-up license** for production

- For Intel Cyclone IV, Cyclone V and Cyclone V SoC. For other device families contact Flexibilis for more information
- For other FPGAs contact Flexibilis for more information
- For price and licensing information contact Flexibilis

3.3 AFEC

The Advanced Flexibilis Ethernet Controller (AFEC) IP provides Ethernet MAC functionalities.

AFEC IP is provided with the following licensing methods:

- **Open Core Plus black-box** design for evaluation
  - For Intel Cyclone IV, Cyclone V and Cyclone V SoC
  - Available from http://www.flexibilis.com/products/downloads/
- **Paid-up license** for production
  - For Intel Cyclone IV, Cyclone V and Cyclone V SoC. For other device families contact Flexibilis for more information
  - For other FPGAs contact Flexibilis for more information
  - For price and licensing information contact Flexibilis

3.4 Interface Adapters

As FRS/FES IP interfaces are GMII there is a selection of additional interface adapters that convert MII/GMII to some other interface type. In general all the adapters provide Avalon interface for configuration and traffic LEDs.

SGMII/1000BASE-X

MII/GMII to SGMII/1000BASE-X adapter is updated and resource optimized version of the older SGMII/1000BASE-X. It provides both Serial Gigabit Media Independent Interface and 1000BASE-X, which can be changed during operation. This adapter does not include any separately licensable Altera IP.

SGMII/1000BASE-X (legacy)

MII/GMII to SGMII/1000BASE-X adapter uses Altera's Triple Speed Ethernet which is a licensable product from Altera. This adapter is provided, but not supported.

1000BASE-X

GMII to 1000base-X provides only 1000BASE-X interface without SGMII support. The resource consumption is even smaller than with the optimized SGMII/1000BASE-X adapter.

RGMII

MII/GMII to RGMII provides support for Reduced Gigabit Media Independent Interface. All interface speeds (10/100/1000 Mbps) are supported.

RMII

MII to RMII provides Reduced Media Independent Interface that supports 10/100 Mbps traffic.

MII

MII to MII provides standard Media Independent Interface. The FRS MII includes some additional signals, which are handled inside the MII adapter.

HPS EMAC

GMII to HPS EMAC can be used in SoC FPGA designs.

I^2C Slave

I^2C to Avalon bridge.

MDIO Slave

MDIO to Avalon bridge.

Licenses

Interface Adapters are provided with the following licensing methods:

- **Open Core Plus black-box** for RGMII, RMII, SGMII/1000BASE-X, 1000BASE-X, 100BASE-FX, I²C Slave
  - For Intel Cyclone IV, Cyclone V and Cyclone V SoC.
  - These blocks are included in the Reference Design package, downloadable from http://www.flexibilis.com/products/downloads/
- **Encrypted license** for MDIO Slave
  - For Intel Cyclone IV, Cyclone V and Cyclone V SoC. For other device families contact Flexibilis for more information
  - This block is included in the Reference Design package, downloadable from http://www.flexibilis.com/products/downloads/
- **Paid-up license** for Adapters
  - For Intel Cyclone IV, Cyclone V and Cyclone V SoC. For other device families contact Flexibilis for more information
  - For other FPGAs contact Flexibilis for more information
  - For price and licensing information contact Flexibilis

3.5 Common Avalon blocks

A group of common Avalon blocks are provided to assist in QSYS designing:

- Avalon Terminate
  - Terminates an Open Avalon Master interface
- Avalon Arbit
  - Combines two Avalon masters i.e. transfers accesses from two slave interfaces to one master interface
- Avalon Export
  - Exports an Avalon interface from a QSYS block
- Avalon Splitter
  - Splits the Avalon address space. Used when the design includes multiple FRS IP Cores

Common Avalon blocks are provided with the following licensing methods:

- **Paid-up license** for Common Avalon blocks
  - Supports any design using an interface that meets Avalon specification
  - These blocks are included in the Reference Design package, downloadable from http://www.flexibilis.com/products/downloads/

3.6 Miscellaneous IP blocks

Flexibilis also provides a group of miscellaneous blocks as listed below:

- Default Clock
  - Can be used instead of FRTC in TC only applications
- GMII Interconnect
  - For QSYS internal connections
- Authentication IF multiplexer
  - For applications with multiple FRS cores using the same security CPLD
- Link Led Control
  - Link LED functionality

FES Reference Design also includes some other miscellaneous IP blocks.

Miscellaneous blocks are provided with the following licensing methods:

- **Encrypted license** for Default clock
  - Included in the Reference Design package, downloadable from http://www.flexibilis.com/products/downloads/
- **Paid-up license** for Miscellaneous blocks
  - Supports any design and vendor

- These blocks are included in the Reference Design package, downloadable from http://www.flexibilis.com/products/downloads/

4 XR7 Software

XR7 is Flexibilis software family. This software is targeted to be used with other Flexibilis products, for example the FES/FRS IPs and XRS chips. Many of these software blocks are not stand-alone but need other software to function correctly so please see the description for each block about its prerequisites.

4.1 XR7 PTP

The XR7 PTP implements IEEE1588-2008 Precision Time Protocol (PTP) [1]. The XR7 PTP supports the following features:

- Ordinary clock (OC, master and slave)
- Boundary clock (BC)
- Peer-to-Peer (P2P) delay measurements
- BMC algorithm
- Asymmetry corrections
- Configurable message intervals
- Support for multiple domains
- Different timescales (PTP, TAI, UTC)
- Layer 3 UDP multicast
- Layer 2 Ethernet multicast
- PTP management protocol (partial, not all messages)

XR7 PTP is provided with the following licensing methods:

- **Paid-up source code** design
  - Available for the following environments:
    - Linux (Debian)
    - NIOS II (no OS)
    - VxWorks
  - For price, licensing and availability or support for different OS, contact Flexibilis

Prerequisites: XR7 PTP is easily portable so it can be used in many systems, for example with the XRS devices, FRS, and FES IPs.

4.2 XR7 Redundancy Supervision

XR7 Redundancy Supervision protocol stack implements HSR/PRP Supervision protocol as specified in IEC 62439-3:2016 [2].

XR7 Redundancy Supervision is provided with the following licensing methods:

- **Paid-up source** code design
  - Available for following environments:
    - Linux (Debian)
    - NIOS II (no OS)
    - VxWorks
  - For price, licensing and availability or support for different OS, contact Flexibilis

Prerequisites: The software can be used with FRS IP or XRS devices.

4.3 XR7 Drivers

The XR7 Drivers are used for example with XRS devices, FES IP, FRS IP, FRTC IP or AFEC IP. XR7 Drivers are needed when developing for Linux, but can also be a useful reference for developing your own drivers when developing for NIOS.

XR7 Drivers are delivered e.g. alongside FES Reference Design for ARM SoC (Chapter 5.2) which can be downloaded here: http://www.flexibilis.com/products/downloads/.

Prerequisites: XR7 Drivers can be used with several different Flexibilis IP blocks.

4.4 XR7 Management Software

This bundle includes four software blocks: XR7 FCM, XR7 IFM, XR7 GUI and XR7 Monitor. These are not sold separately.

- XR7 FCM (Flexibilis Configuration Manager Module and Daemon)
  - XR7 FCM is an implementation of IETF NETCONF [3] network management protocol. FCM design is modular. The daemon itself implements the protocol. The FCM modules, implemented as dynamically linked shared object libraries, provide NETCONF support for specific system components like XR7 PTP, XR7 Redundancy Supervision, network interfaces and so on.
- XR7 IFM (Interface Manager)
  - XR7 IFM is a daemon which provides NETCONF support for various network interfaces. Its design is modular – each module is implemented as a dynamically linked shared object library implementing XR7 FCM module interface.
- XR7 GUI (Graphical User Interface)
  - XR7 GUI provides web interface to the device for presenting status information and for configuring the system as desired by user. It is implemented as a Java servlet and it uses NETCONF to access the device resources.
- XR7 Monitor
  - XR7 Monitor provides a NETCONF interface for device HW and SW identification and version information. It does not provide any configuration settings.

XR7 Management Software is provided with the following licensing methods:

- **Paid-up source** code design
  - Available for following environments:
    - Linux (Debian)
  - For price, licensing and availability or support for different OS, contact Flexibilis

Prerequisites: XR7 PTP or XR7 Redundancy Supervision software are needed.

4.5 XR7 Firmware Configurator

XR7 Firmware Configurator is used to control FES Reference Design over Ethernet. XR7 Firmware Configurator includes:

- Protocol specification and library
- Implementation for NIOS II
- Test tool for Linux

XR7 Firmware Configuration is provided with the following licensing methods:

- **Paid-up source** code design
  - Available for the following environments:
    - NIOS II (no OS)
  - For price, licensing and availability or support for different OS, contact Flexibilis

Prerequisites: XR7 Redundancy Supervision and FES Reference Design for NIOS are needed. Can be used with FRS IP.

4.6 XR7 Software Platform

XR7 Software Platform is a complete system for building and managing GNU/Linux based firmware for devices. Devices can vary from more or less standard server PCs, embedded systems with a SoC to virtual machines. The platform is based on Debian and uses various Debian utilities and conventions. However, it uses them in a more specific way and presents an easy to use interface to them without sacrificing flexibility.

The Platform is available as a disk image, which can be used to setup multiple networked machines as needed. Machines can have a different firmware management related roles or overlapping roles but one machine acts as a software package repository server.

XR7 Software Platform provides the following features and services:

- Building software packages
  - Building software package means taking source code and compiling and linking it to binaries that can be used on target device. Cross-compiling is used when needed. Also files that do not need compiling can be packaged. Platform offers simple way to build packages either for testing during development or to be included in the firmware. Packages are built in robust, reliable, and reproducible way.
- Building device firmware
  - Firmware contains all software needed in a target device, in some target device specific format. Examples are SD-card images, NAND flash filesystem images, and so on. Platform offers simple way to create releases and needed firmware files. Detailed contents of each release are available and also accessible via HTTP using simple URLs.
- Small firmware upgrade packs
  - In many cases it is not desirable to replace the whole firmware on SD-card or NAND flash memory when doing system upgrades. Platform offers simplified way to create small upgrade packs, which provide new or upgraded packages or remove unneeded software packages from the firmware. Full customization of upgrade installation process is possible.
- Updating firmware of test system
  - Typically there are some devices in a dedicated test system or in lab. Platform offers a simple way to keep devices up-to-date by downloading and installing needed software from package repository server.
- Local Debian package archive
  - Platform manages software as Debian packages (.deb files). The package repository server acts as a local Debian package archive for upstream (Debian and Flexibilis) software as well as project specific software. New and upgraded software is sent to the package archive via SSH, and packages are available from the repository via HTTP. Many debugging and diagnostics utilities from Debian are available for use in test system devices, without needing to be included in official firmware.
- HTTP server
  - Package archive functionality uses HTTP, so Apache HTTP server is included in the platform. In each machine the HTTP server can also be used to configure other firmware related custom tasks.
- Continuous Integration (CI) server
  - Platform contains Jenkins CI server that can be used as needed. Its use is not required. Also external CI servers can be used for various firmware management tasks.
- DNS server
  - Typically there already is a DNS server for the development network and often it's best to use it to give names for platform servers (the package archive server, HTTP server virtual hosts). In some cases it may not be possible or desirable, so BIND DNS server is included with the platform.
- Multiple developer support
  - Many developers can use a single platform machine, or each developer can use his own machine. Any combination is also possible.

XR7 Software Platform is provided with the following licensing methods:

- **Paid-up source** code design
  - Available for the following environments:
    - Linux (Debian)
  - For price, licensing and availability or support for different OS, contact Flexibilis

Prerequisites: -

5 FES Reference Designs

Flexibilis provides Switch IP Reference Designs for evaluating the FES and FRS IPs. Mainly the reference designs can be divided into two categories: Reference designs for NIOS and reference designs for ARM SoC.

5.1 FES Reference Design for NIOS

Reference Design for NIOS is provided for the following evaluation boards:

- Cyclone IV GX, DK-DEV-4CGX150N [4]
- Cyclone V GX, DK-DEV-5CGXC7NES [5]
- Cyclone V GT, DK-DEV-5CGTD9N [6]

The Reference design includes:

- Reference design **image** (flash file) including
  - FRS IP, time limited operation
  - AFEC IP
  - FRTC IP
  - NIOS with
    - XR7 PTP
    - XR7 Redundancy Supervision
    - XR7 Firmware Configuration
    - Design related control SW
  - FRS related FPGA blocks (Interface adapters, Avalon bus components etc.) For more information check the Reference design specification
- Design related control SW **source codes** (component “drivers”, initializations etc.)
- FRS related FPGA blocks: part as **black-box** and the rest as **source codes** (Interface adapters, Avalon bus components etc.)
- Quartus Project files

Note: The reference design package does not include FRS IP, AFEC IP, FRTC IP or SW protocol stacks. To be able to recompile the design, these items are needed. The Reference design flash file can be used to configure the FPGA on the evaluation board.

5.2 FES Reference Design for ARM SoC

Reference design for ARM is provided for the following evaluation boards:

- Altera Cyclone V SoC Development kit, DK-DEV-5CSXC6N [7]
- Terasic Cyclone V SoC Development kit [8]

Reference design includes:

- Reference design **image** (SD card image) including
  - FRS IP, time limited operation
  - FRTC IP
  - Linux with
    - XR7 PTP
    - Flexibilis Redundancy Supervision
    - FCMs
    - Interface Managers
    - XR7 GUI
    - Kernel drivers
  - FRS related FPGA blocks (Interface adapters, Avalon bus components etc.) For more check the Reference design specification
- Kernal drivers, **source codes**
- FRS related FPGA blocks: part as **black-box** and the rest as **source codes** (Interface adapters, Avalon bus components etc.)
- Quartus Project files

- Note: The reference design package does not include FRS IP, AFEC IP, FRTC IP, SW protocol stacks, FCM, Interface manager or XR7 GUI. To be able to recompile the design, these items are needed. The Reference Design SD card image can be used to boot Linux and configure the FPGA on the evaluation board.

6 Services

Flexibilis provides services related to our products and core competences.

6.1 Customer Portal

In Customer Portal Flexibilis provides support related to our products and services. Also all documentation related to our products is available in the Portal. The Portal requires registration and is open to all Flexibilis customers. All service requests are public and therefore other users can also see them. However, the questions are anonymous so other users cannot see customer's identity or profile information.

Account can be created here: http://www.flexibilis.com/customer-portal/

6.2 Premium Support

Flexibilis also offers Premium Support in the Customer Portal. Premium Support is a personal service with shorter response time. Other users cannot see customer's service requests and the questions will not be published. For pricing and details, please contact Flexibilis.

6.3 Getting Started with FRS – Training Sessions

"Getting Started with FRS" are training sessions directed to those who plan to implement FRS and HSR, PRP or IEEE 1588. The training decreases time-to-market, reduces technical risk and makes the implementation of FRS smoother. The training consists of three online sessions, each lasting from 1 to 3 hours. For more information, see: https://www.flexibilis.com/getting-started-with-frs/

6.4 Integration and Design Services

Flexibilis can help customers to integrate our products and technologies with customer's system, which will make the implementation easier as well as save valuable time. We also offer FPGA design and embedded software design services (for Linux).

7 Product Matrix

The Product and availability matrix based on provided functionality is presented in Table 1.

Table 1. Product Matrix based on provided functionality

	Quick Evaluation	Limited Design Evaluation and Development	Full Functionality
FPGA IP Cores			
Standard FES IP		C	E F
FRS IP	A	C	E F
FRTC IP	A B	C	E F
AFEC IP	A	C	E F
Interface Adapters	A B	C	E F
XR7 Software			
XR7 PTP	A B		F
XR7 Redundancy Supervision	A B		F
XR7 Drivers	B		D
XR7 Management	B		F
XR7 Firmware Configurator	A		F
XR7 Software Platform			F

A	Reference Design Flash File. Downloadable from www.flexibilis.com/products/downloads
B	Reference Design SD Card Image. Downloadable from www.flexibilis.com/products/downloads
C	Time-limited, free of charge Evaluation version available from www.flexibilis.com/products/downloads
D	Full functionality part of the reference design packages. Downloadable from www.flexibilis.com/products/downloads
E	Paid-up black box. Contact Flexibilis.
F	Paid-up source code. Contact Flexibilis.

8 Abbreviations

Term	Description
AFEC	Advanced Flexibilis Ethernet Controller
CPU	Central Processing Unit
FCM	Flexibilis Configuration Manager
FPGA	Field Programmable Gate Array
FES	Flexibilis Ethernet Switch
FRS	Flexibilis Redundant Switch
FRTC	Flexibilis Real Time Clock
GMII	Gigabit Media Independent Interface
HSR	High-availability Seamless Redundancy
MAC	Media Access Controller
MII	Media Independent Interface
PPS	Pulse Per Second
PTP	Precision Time Protocol
PRP	Parallel Redundancy Protocol
SD	Secure Digital
TSN	Time-sensitive Networking

9 References

[1] IEEE standard 1588-2008

[2] Standard IEC 62439-3:2016

[3] NETCONF, RFC 4741, http://tools.ietf.org/html/rfc4741

[4] Cyclone IV GX FPGA Development Kit from Altera (ordering code DK-DEV-4CGX150N): http://www.altera.com/products/devkits/altera/kit-cyclone-iv-gx.html

[5] Cyclone V GX FPGA Development Kit from Altera (ordering code DK-DEV-5CGXC7NES): http://www.altera.com/products/devkits/altera/kit-cyclone-v-gx.html

[6] Cyclone V GT FPGA Development Kit from Altera (ordering code DK-DEV-5CGTD9N): http://www.altera.com/products/devkits/altera/kit-cyclone-v-gt.html

[7] Altera Cyclone V SoC Development kit, http://www.altera.com/products/devkits/altera/kit-cyclone-v-soc.html

[8] Terasic Cyclone V SoC Development kit, http://www.terasic.com.tw/cgi-bin/page/archive.pl?CategoryNo=167&No=816