FRTC

User Manual

Rev	Date	Author	Comments
0.1	4.9.2007	Flexibilis Oy / Sami Muurinaho	First version
1.0	21.12.2010	Flexibilis Oy / Timo Koskiahde	Updates and approved.
1.1	8.8.2011	Flexibilis Oy / Janne Kaattari	Complete register description.
1.2	12.9.2012	Flexibilis Oy / Jouni Kujala	PPS output added.
1.3	11.3.2015	Flexibilis Oy / Jouni Kujala	Changed the register map to comply with the implementation. Added a chapter for Generics.
1.4	18.3.2015	Flexibilis Oy / Jouni Kujala	Subnanoseconds value removed from CUR_NSEC register.
1.5	21.9.2015	Flexibilis Oy / Jarkko Ruoho	Added DEFAULT_STEP_NS and DEFAULT_STEP_SNS generics. Changed SUBNSEC_WIDTH value to support 0..16 (both sides inclusive). Nanosecond time adjustment is not summed to nanosecond step anymore
1.6	14.12.2015	Flexibilis Oy / Jarkko Ruoho	Added note about adjustments possibly breaking PPS pulse. Added info about PPS offset.

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1 About This Document

This is a user manual for Flexibilis Real-Time Clock (FRTC) Intellectual Property (IP) block. FRTC IP can be used to provide wall clock time for other IPs. The time format is compatible with the time format defined in IEEE1588 standard [1], so it can be used for example to provide time for IEEE1588 compatible IP blocks.

The register descriptions in this document follow these rules: Unless otherwise stated, all the bits that activate or enable something are active when their value is 1 and inactive when their value is 0. The explanation of the bit types is the following:

- RO = Read Capable Only. The bits marked with RO can be read. Writing to these bits is allowed if not otherwise stated. If writing is allowed, it does not affect the value of the bit.
- R/W = Read and Write capable. The bits can be read and written. Writing 1 to the bit makes its value 1. Writing 0 to the bit makes its value 0.
- R/SC = Read, Write and Self Clear. The bits can be read and written. Writing 0 to the bit does nothing. Writing 1 to the bit makes its value 1 for a while, but after that the value automatically returns back to 0.

The bits marked as *Reserved* should not be written anything but 0, even if they are marked as read capable only, because their function may change in future versions.

Bit and byte order used for 16, 32 and 64 registers is depicted in Figure 1.

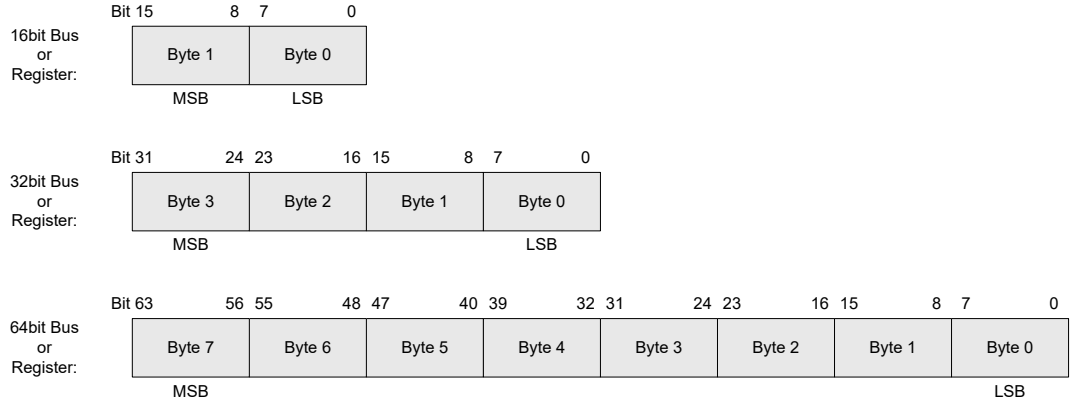

Figure 1. Bit and Byte Order

Signal names are written in document with `SignalName` style. Block names are written with Capital first letter. Pseudo code is written with `PseudoCode` style and command line commands are written with `CommandLine` style.

Chapter 2 defines the IP functionality, Chapter 3 contains abbreviations and Chapter 4 references.

2 Functionality

FRTC has an Avalon Memory Mapped slave interface and one or more time interfaces. The Avalon interface is used by controlling entity (for example host CPU) to read and adjust the internal time or FRTC. The Time interface(s) provide time information for other IP blocks. [Figure 2]

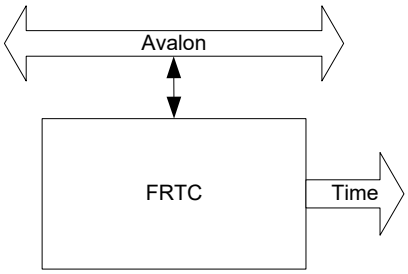

Figure 2. FRTC Interfaces

FRTC has two clock domains, one for Avalon interface and another for calculating time. This way different clocks can be used in Avalon bus and calculating the wall clock time.

In case of FRTC time is presented in seconds and nanoseconds. Time interface supports a 96 bit time format compatible with IEEE1588, which defines 48 bits for seconds, 32 bits for nanoseconds and 16 bits for subnanoseconds.

FRTC is implemented with an NCO (Numerically Controller Oscillator) that counts nanoseconds. Seconds value is updated and nanoseconds value wraps around always when nanoseconds value exceeds 1 000 000 000 (corresponds to one second). Because of this, the nanoseconds value can never be more than 30 bits.

Note that the number of time interfaces and the number of bits used to present sub-nanosecond are compile time parameters (VHDL generics).

NCO starts counting when step is configured. If DEFAULT_STEP_NS and DEFAULT_STEP_SNS are zero, step configuration is done with register write to STEP_SIZE and TIME_CMD registers. TIME_CMD register must be used also for time adjustment and time read operations.

2.1 Registers

Registers of FRTC are presented in Table 1.

Address	Register	Description
0x00000000	GENERAL	<u>General</u> – Reset: 0 x 00 00 00 00 80 00 90 XX Contains FRTC version information and general control bits. Bits 7-0 : RO Revision ID *ID number that is incremented when HW or SW interface of the IP core is changed.* Bits 23-8 : RO Device ID *0x90: FRTC* Bits 63-24 : RO *Reserved*
0x00000008 … 0x00000FF8	*Reserved*	*Reserved*
0x00001000	CUR_NSEC	<u>Current time nanoseconds</u> – Reset: 0 x 00 00 00 00 00 00 00 00 – Updated with Read Time command *(see TIME_CMD register).* Bits 31-0 : RO *Reserved* Bits 61-32 : RO Nanoseconds *Nanoseconds part of the current time.* Bits 63-62 : RO *Reserved*
0x00001008	CUR_SEC	<u>Current time seconds</u> – Reset: 0 x 00 00 00 00 00 00 00 00 – Updated with Read Time command *(see TIME_CMD register).* Bits 47-0 : RO Seconds *Seconds part of the current time.* Bits 63-48 : RO *Reserved*
0x00001010	TIME_CC	<u>Clock cycle counter</u> – Reset: 0 x 00 00 00 00 00 00 00 00 – Free-running counter running with *time_clk*. – Updated with Read Time command *(see TIME_CMD register).* Bits 47-0 : RO Free-running clock cycle counter *Clock cycles since the reset. The value wraps around automatically. Time adjustments have no effect on this value.* Bits 63-48 : RO *Reserved*
0x00001018	*Reserved*	*Reserved*
0x00001020	STEP_SIZE	<u>NCO step size</u> – Reset: Depends on generic settings. – NCO step size. This value is added to the internal NCO at every clock cycle. Defines the speed of the clock time. Bits 31-0 : R/W Subnanoseconds *Subnanoseconds step size for NCO. The new value is taken into use with Adjust Step command (see TIME_CMD register).* Bits 37-32 : R/W Nanoseconds *Nanoseconds step size for NCO. The new value is taken into use with Adjust Step command (see TIME_CMD register).* Bits 63-38 : RO *Reserved*
0x00001028	*Reserved*	*Reserved*
0x00001030	ADJUST_NSEC	<u>Adjust time (nanoseconds part)</u> – Reset: 0 x 00 00 00 00 00 00 00 00 – This value is added to nanoseconds part with Adjust Time command instead of STEP_SIZE nanoseconds. For change to take effect TIME_CMD register must be written also. The nanosecond adjustment value is unsigned and therefore always positive. To go backwards use negative seconds adjustment (ADJUST_SEC register). For example, to go 500 ns backward, adjust 999 999 500 ns forward and one second backward. – Allowed range for nanosecond adjustment is from 0 to 999 999 999 – PPS output signal functionality is not specified if adjustments are used during normal operation. The PPS pulse may be wrong length or missing. Bits 31-0 : RO *Reserved* Bits 61-32 : R/W Nanoseconds Bits 63-62 : RO *Reserved, always write zero*
0x00001038	ADJUST_SEC	<u>Adjust time (seconds part)</u> – Reset: 0 x 00 00 00 00 00 00 00 00 – This value is added to seconds part with Adjust Time command (see TIME_CMD register). The seconds adjustment value is signed and can therefore be also negative. To go backwards, use two's complement arithmetic's. Bits 47-0 : R/W Seconds *The highest bit (bit 47) is the sign.*

		Bits 63-48 : RO *Reserved*
0x00001040	TIME_CMD	Time command register – Reset: 0 x 00 00 00 00 00 00 00 00 Bit 0 : R/SC Adjust Time *Adds (for one time only) the values in ADJUST_NSEC and ADJUST_SEC registers to internal time (NCO).* Bit 1 : R/SC Adjust Step *Take the new values in STEP_SIZE register into use.* Bit 2 : R/SC Read Time *Updates the CUR_NSEC, CUR_SEC and TIME_CC registers with the current values in the NCO* Bits 63-3 : RO *Reserved*

Table 1. FRTC Registers

2.2 Generics

The compile time configuration is presented in Table 2.

Generic name	Default value	Description
RST_ACTIVE	1	Active edge of reset signal. The allowed values are 0 (active low) and 1 (active high).
SUBNSEC_WIDTH	0	Number of bits for subnanoseconds (parts of a nanosecond). Allowed values 0…16.
EXT_PORT_HIGH	0	Number of Time interfaces minus one.
DEFAULT_STEP_NS	0	Default value for the step nanosecond value after hw reset
DEFAULT_STEP_SNS	0	Default value for the step subnanosecond value after hw reset

Table 2. FRTC Generics

2.3 External Signals

FRTC has two kinds of external interfaces: one Avalon interface and 1…N Time interfaces. Avalon interface is defined in Altera specifications. Time interface together with general signals is specified in Table 3.

Name	Direction	Description
rst	Input	Reset Block reset
clk	Input	Clock Clock used by Avalon interface.
time_rst	Input	Time Reset Resets time counting.
time_clk	Input	Time Clock Clock used in time counting and time interface.
time_req(0:0)	Input	Transmit Time Request This signal toggles to request new time. This signal is synchronous to the time_clk signal.
time_ack(0:0)	Output	Transmit Time Acknowledge This signal shall toggle to follow the time_req signal when data is updated on the time_data(95:0) signal. This signal is synchronous to the time_clk.
time_data(0:95)	Output	Time Data 96 bit time format with 48 bits for seconds, 32 bits for nanoseconds and 16 bits for subnanoseconds. Updated when time_ack is active.
PPS	Output	Pulse Per Second PPS pulse of 20 us in length. The rising edge is two clock cycles after the nanoseconds value in the NCO wraps around. Falling edge is equally accurate: 20 us and two clock cycle after the NCO wraps around. Time adjustments may cause invalid length or completely missing pulse.

Table 3. FRTC External Signals (with one time interface)

3 Abbreviations

Term	Description
CPU	Central Processing Unit
FPGA	Field Programmable Gate Array
IEEE	Institute of Electrical & Electronics Engineers
IP	Intellectual Property
NCO	Numerically Controlled Oscillator

4 References

[1] IEEE Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems, IEEE Std. 1588-2008.