SpeedChip XRS7000E Reference Board

User Manual

The XRS7003 and XRS7004 are HSR and PRP (IEC 62439-3 Clause 5 & 4) enabled single-chip gigabit Ethernet switches. XRS7003 can be employed in HSR and PRP End-nodes and XRS7004 in both End-Nodes and HSR and PRP RedBoxes. A QuadBox can be built using two XRS7004 devices.

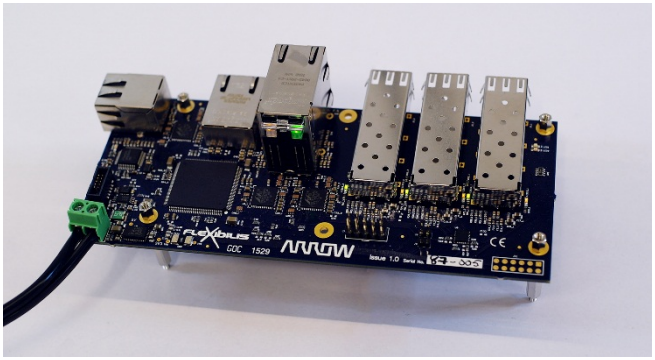
This document is a user manual for XRS7000E Reference Board.

Board Features

- XRS7004E Ethernet switch chip
- Three 10/100/1000 Mbit/s Full-Duplex Twisted pair copper Ethernet interfaces with RJ45 connectors
- Three SFP cages for fiber optic Ethernet modules (100/1000 Mbit/s)
- 10/100 Mbit/s CPU port with RJ45 connector
- I^2C and MDIO interfaces for accessing XRS7000 registers
- PPS (Pulse per Second) input and output for time synchronization
- 5 V input power
- Designed to be compatible with Raspberry Pi single-board computer. (SW package for Pi available)

High-availability Seamless Redundancy and Parallel Redundancy Protocol

HSR and PRP protocols are used in applications that require short reaction time and high availability. Typical applications include smart grid electrical substation automation and other critical networking applications such as industrial automation, motion control, vehicle and military communication. HSR and PRP provide a network that has no single point of failure and zero recovery time in case of a failure: Single network faults will not result in any frame loss. The network is fully operational even during maintenance as any network device can be disconnected and replaced without breaking the network connectivity.



Contents

Figures

Tables

Five Years Out

Revision History

Rev	Date	Comments
1.0	16.2.2016	First release
1.1	19.4.2016	Board Ordering Number updated

Flexibilis Oy retains the right to make changes to this document at any time, without notice. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document. Flexibilis Oy makes no warranty of any kind, expressed or implied, with regard to any information contained in this document, including, but not limited to, the implied warranties of merchantability or fitness for any particular purposes. Further, Flexibilis Oy does not warrant the accuracy or completeness of the information, text, graphics, or other items contained within this document. Flexibilis Oy assumes no responsibility or liability whatsoever, and Flexibilis Oy disclaims any express or implied warranty, relating use of SpeedChip XRS7000 Reference Board liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright or other intellectual property right.

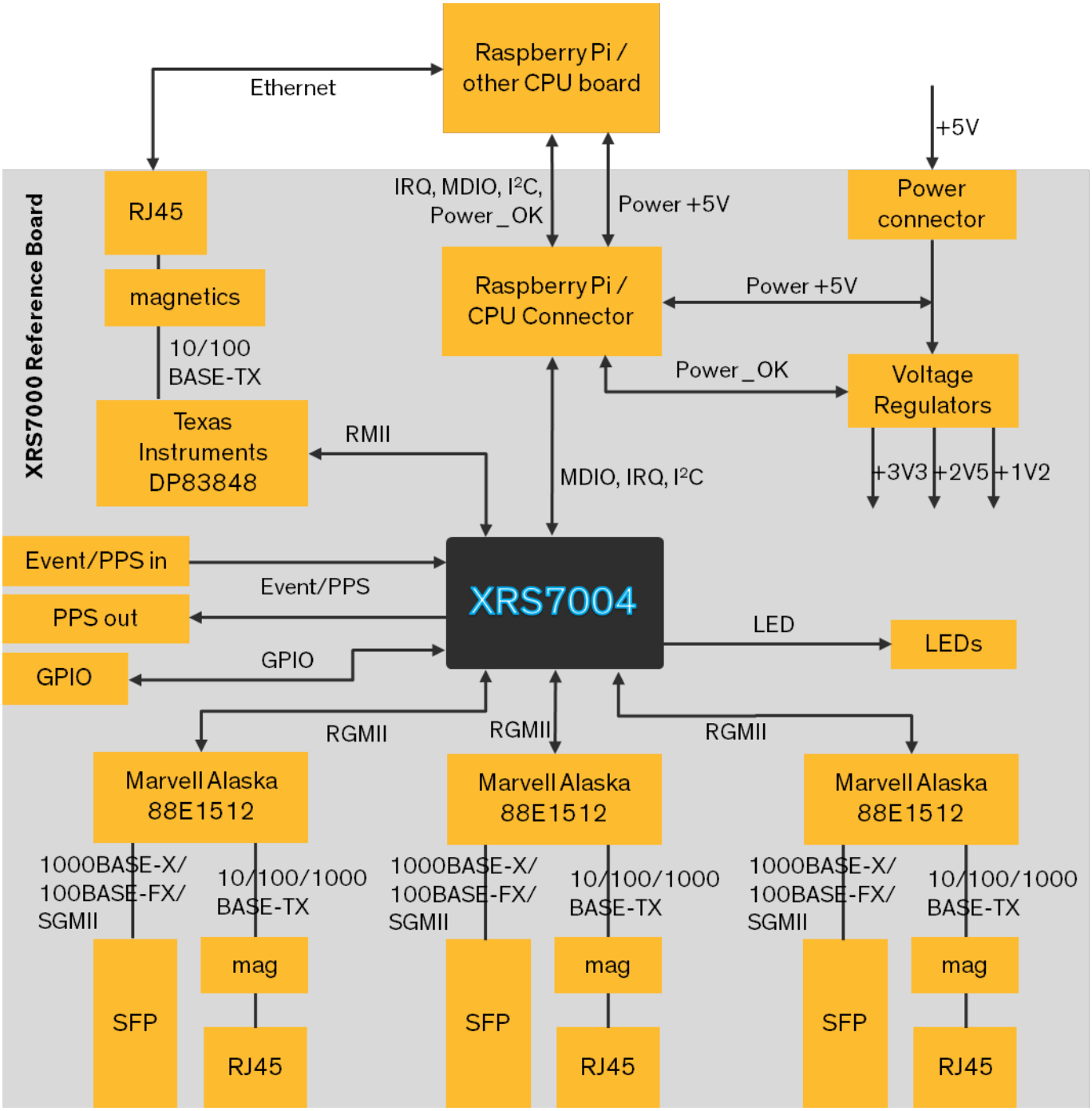
© Copyright Flexibilis Oy 2016. All rights reserved.
All trademarks are the property of their respective owners.

1. FUNCTIONAL OVERVIEW

The main components of the board are presented in Figure 1. The most important component on the board is the XRS7004 chip whose main job is to forward Ethernet frames between the board's Ethernet interfaces.

The functionality of the XRS7004 chip is controlled using either MDIO or I^2C interface. For controlling the XRS7004 chip a CPU board has to be connected to the CPU connector of the board. The CPU connector is designed to be pin compatible with Raspberry Pi credit card size single board computer. Attaching to other kinds of CPU boards is possible using a custom made cable. Note that accessing the on-board PHYsical layer chips (Marvell 88E1512 and TI DP83848) happens using MDIO and accessing SFP modules happens using I^2C, so full control of the board requires using both MDIO (Chapter 1.1) and I^2C (Chapter 1.2) with the CPU board.

Figure 1. Board Block Diagram



1.1 MDIO

The MDIO buses of the board are presented in Figure 2. MDIO is used for the CPU to access the registers of the four PHY devices on the board and the registers of the XRS chip. Marvell 88E1512 PHY devices have only two options for possible MDIO addresses, which means that it is not possible to have three 88E1512 devices on the same MDIO bus. The MDIO addresses are presented in Table 1. The maximum frequency of the I²C clock is 400 kHz.

Figure 2. MDIO

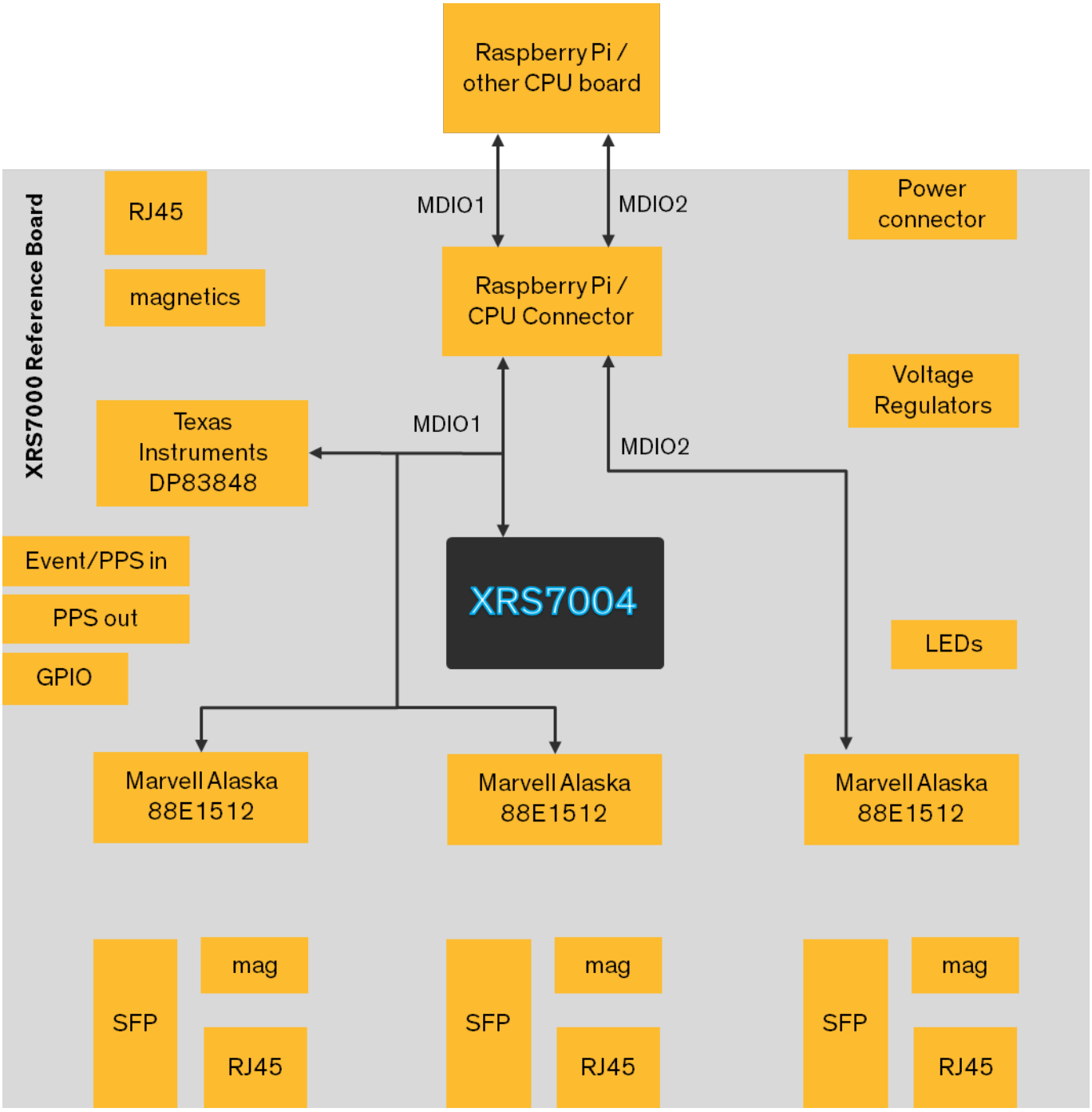


Table 1. MDIO addresses

MDIO bus	Device	MDIO Address
MDIO1	XRS7004	8
MDIO1	TI DP83848	5
MDIO1	Marvell 88E1512, port1	1
MDIO1	Marvell 88E1512, port2	0
MDIO2	Marvell 88E1512, port3	1

Five Years Out

1.2 I²C Bus

The CPU can use the I²C bus to access the registers of XRS7004 and the SFP modules. With I²C access to XRS7004 the register map of XRS7004 looks the same as with MDIO, and exactly the same functionality is available. The maximum frequency of the MDIO clock is 2.5 MHz.

For controlling the SFP modules the I²C bus is connected to NXP semiconductor PCAL9555A IO expander chip. This IO expander then provides control signals for SFP modules including an own I²C bus for each module, see Table 2.

Table 2. SFP Module Control Signals

SFP Cage	SFP Signal	PCAL9555A IO
1	TX Fault	P0_0
1	MOD-DEF2 (I²C data)	P0_1
1	MOD-DEF1 (I²C clock)	P0_2
1	MOD-DEF0 (present)	P0_3
1	LOS	P0_4
2	TX Fault	P0_5
2	MOD-DEF2 (I²C data)	P0_6
2	MOD-DEF1 (I²C clock)	P0_7
2	MOD-DEF0 (present)	P1_0
2	LOS	P1_1
3	TX Fault	P1_2
3	MOD-DEF2 (I²C data)	P1_3
3	MOD-DEF1 (I²C clock)	P1_4
3	MOD-DEF0 (present)	P1_5
3	LOS	P1_6
-	-	P1_7

The on-board I²C connections are presented in Figure 3 and I²C addresses are presented in Table 3.

Five Years Out

Figure 3. I²C

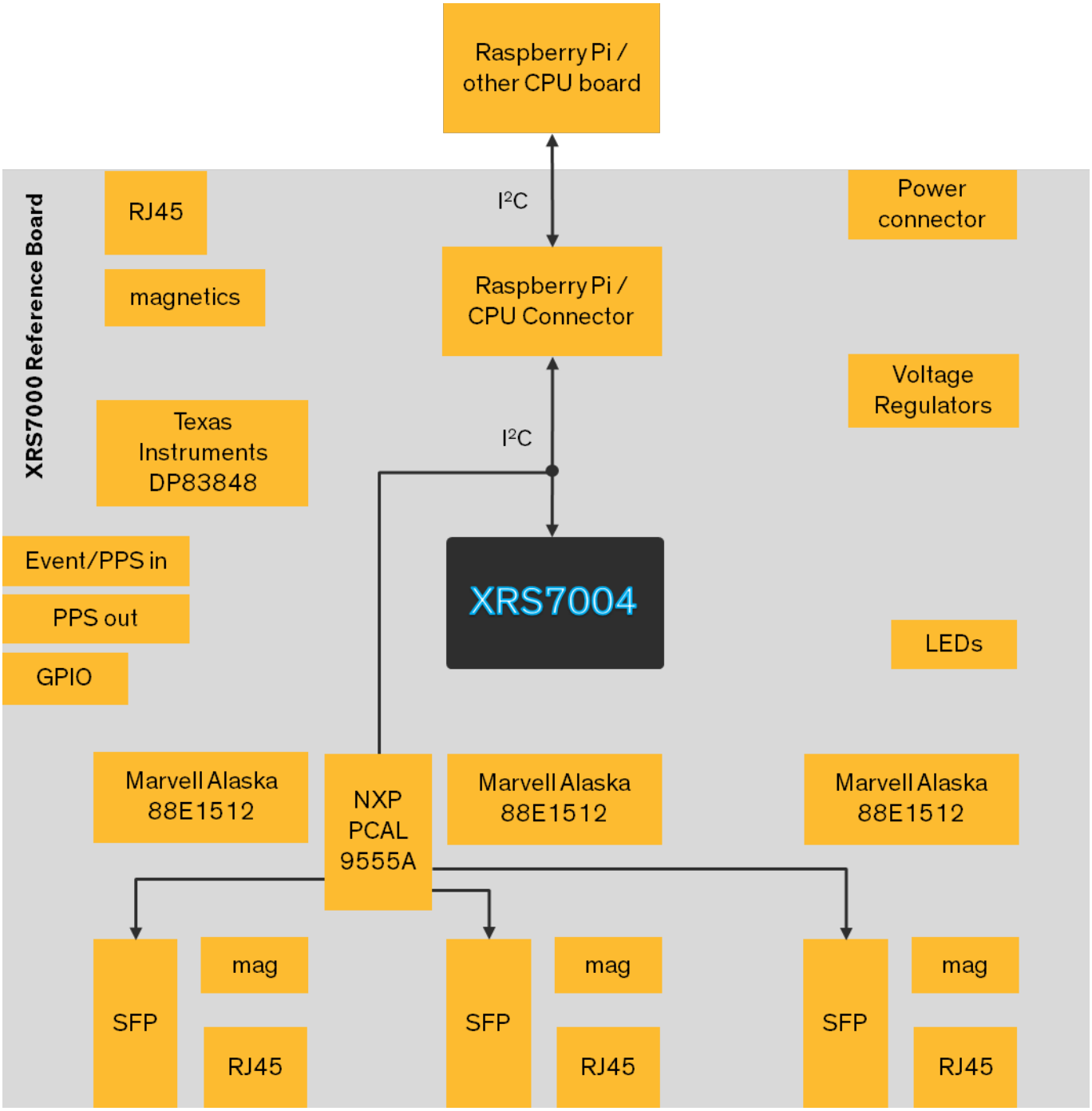


Table 3. I²C addresses

Device	I²C Address
XRS7004	0x24
IO expander NXP PCAL 9555A (for SFP modules)	0x20

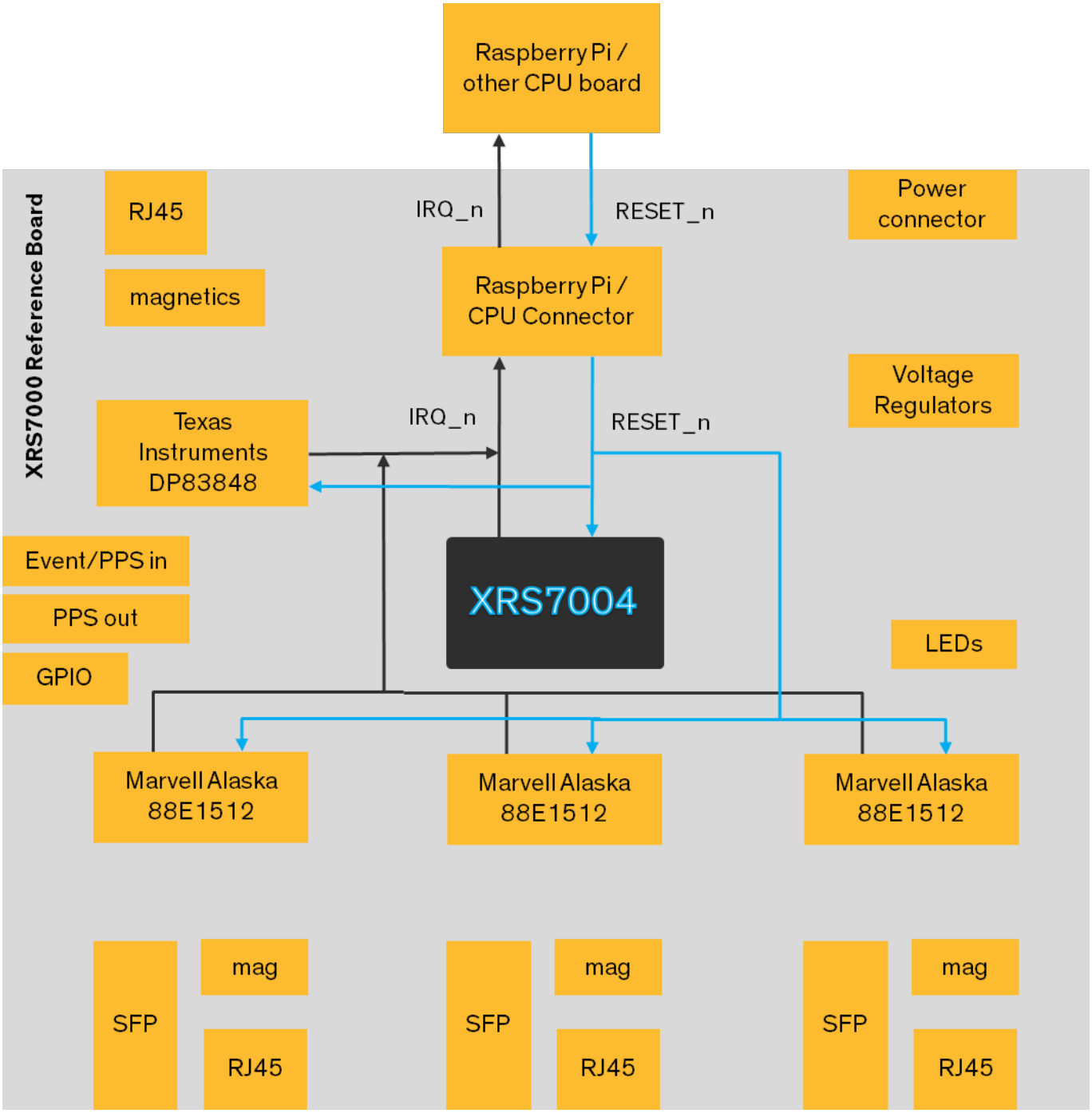
Five Years Out

1.3 Reset and Interrupt

The on-board reset and IRQ lines are presented in Figure 4. Both reset and IRQ are active low. The interrupt request is open drain wired-OR.

The CPU needs to activate and deactivate the reset signal after power-up before configuring the XRS7004 and the PHYs. Usage of the interrupt request line is optional.

Figure 4. Reset and Interrupt



Five Years Out

2. INTERFACE DESCRIPTIONS

The interfaces of the board are presented in Figure 5 and Figure 6. The red circles of Figure 6 indicate the first pin.

Figure 5. Connector Locations

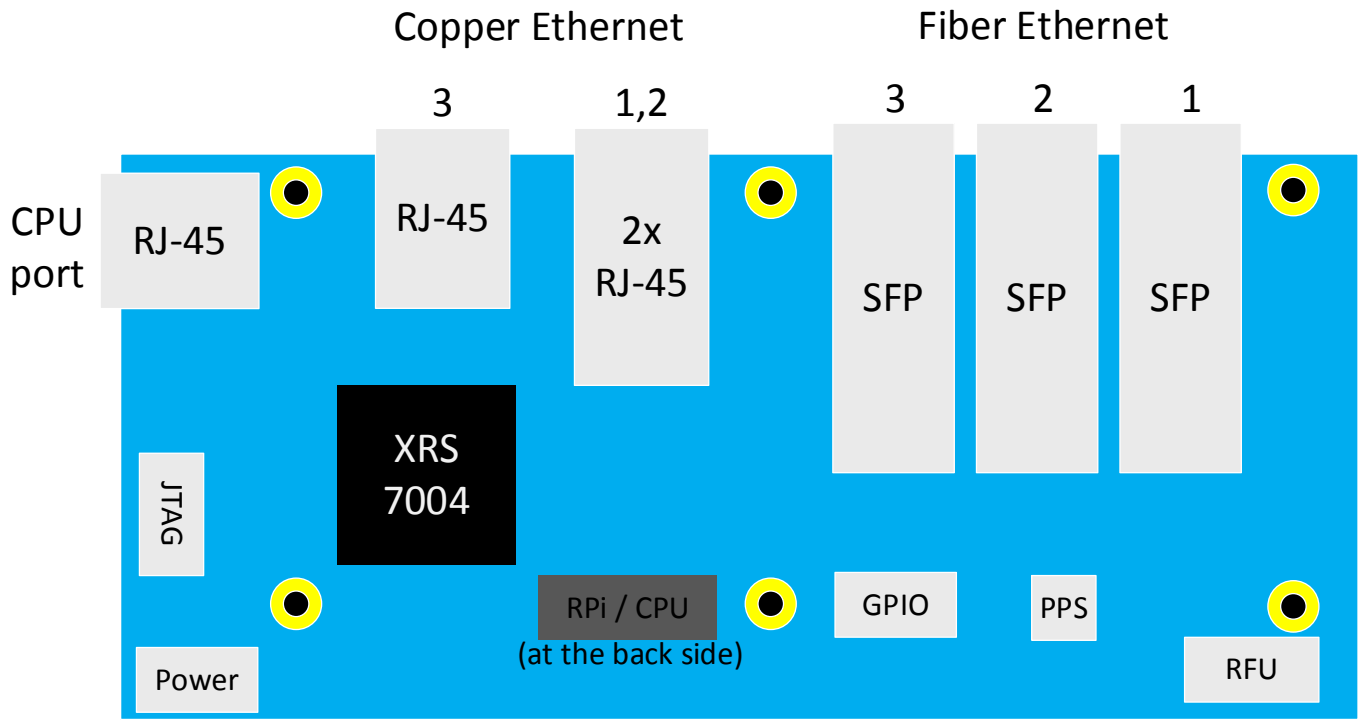
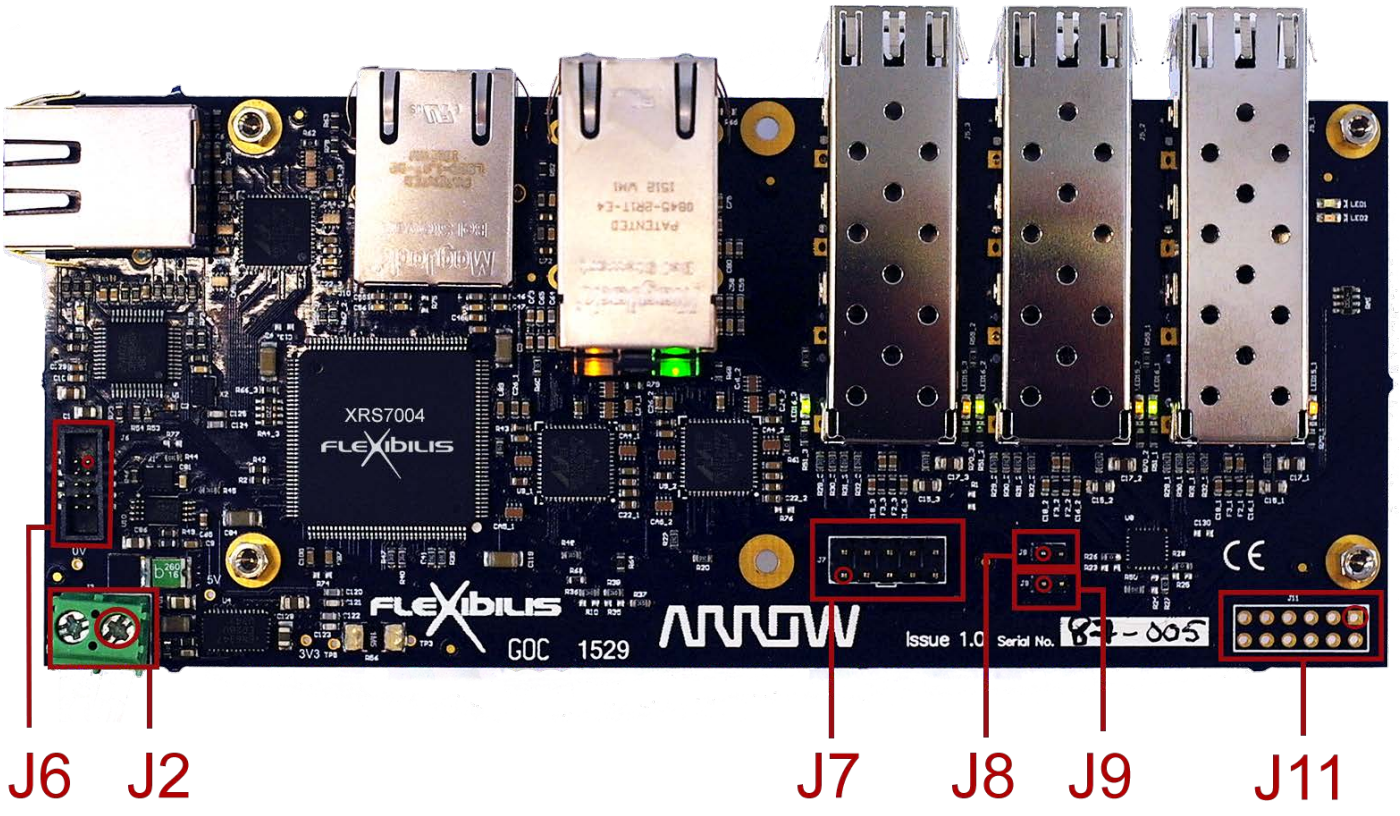


Figure 6. Connector Pin 1 Locations

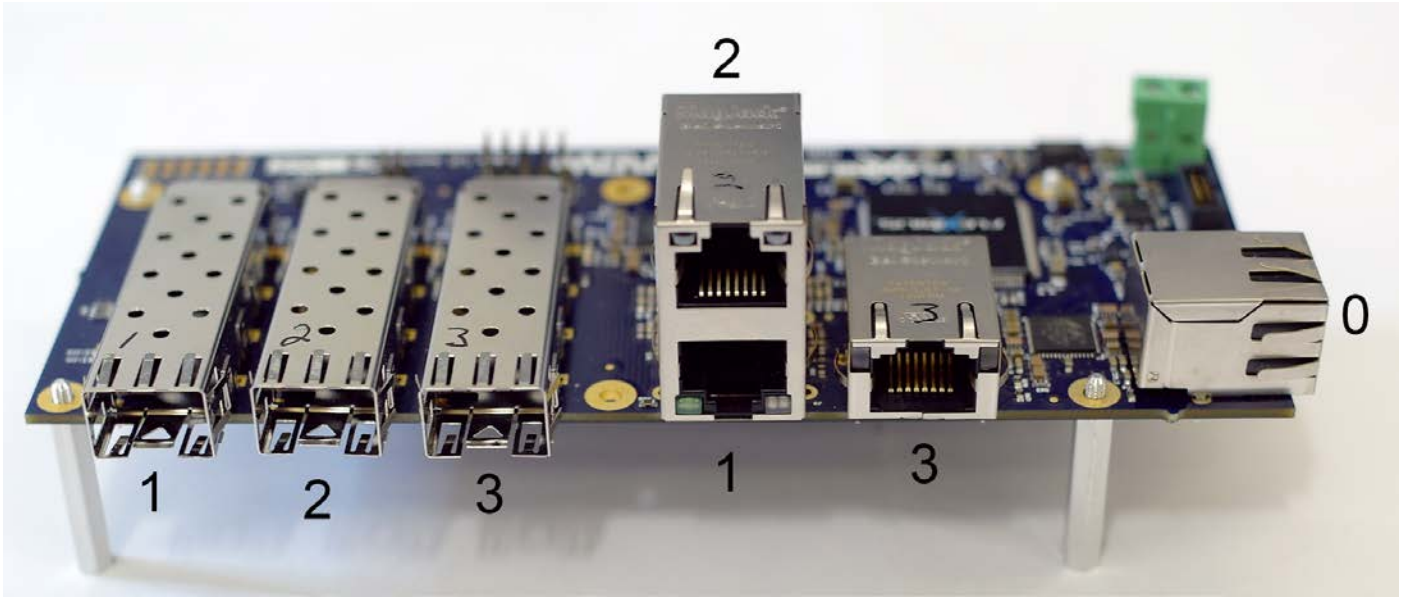


ARROW FLEXIBILIS
Five Years Out

2.1 Copper Ethernet

Copper Ethernet interfaces 1, 2 and 3 are provided with standard RJ45 connectors. They support 10 Mbit/s, 100 Mbit/s and 1000 Mbit/s interface speeds. The interfaces support auto crossover and auto negotiation, but no PoE.

Figure 7. Ethernet Ports



2.1.1 *CPU Port*

The CPU port (port 0 in Figure 7) is a standard RJ45 Ethernet port that supports 10 Mbit/s and 100Mbit interface speeds. The interface is meant for the host CPU to be able to send and receive Ethernet frames to/from the network, to be used for example for Time Synchronization (IEEE 1588 PTP), HSR/PRP supervision, web interface and SSH server functionalities running on the CPU board.

2.2 SFP

Fiber Ethernet is provided with SFP (Small Formfactor Pluggable) fiber optic modules. Also SFP copper Ethernet modules are supported.

An SFP interface cannot be used at the same time with the corresponding copper Ethernet interface (Chapter 2.1). The priority order of the SFP and copper Ethernet interfaces is software configurable by writing into PHY chip registers.

Five Years Out

2.3 Power

Operating power for the board is provided to the screw connector J2 (see Table 4). Alternatively the board can take its power from the CPU connector. The screw connector (J2) power pin and the CPU connector +5 V power pins are connected to each other via 2.6 A fuse and the current may flow to either direction.

Table 4. Power Connector (J2) Pinout

Connector Pin	Function
1	+5 V in
2	GND

Do not feed power to the board using both CPU connector AND Power Connector (J2) at the same time.

2.4 CPU

The connector for CPU board (J4, see Figure 8) is compatible with Raspberry Pi (both pinout and placement). The connector can be used for powering the CPU Board from XRS7000 Reference Board, or for powering the XRS7000 Reference Board from the CPU Board if the CPU board uses +5 V power input (like Raspberry). The pinout of the CPU connector is presented in Table 5. The I/O voltage is 3.3 V.

The inputs are not 5 V tolerant.

Figure 8. CPU/RPi Connector (J4) Pin 1 Location

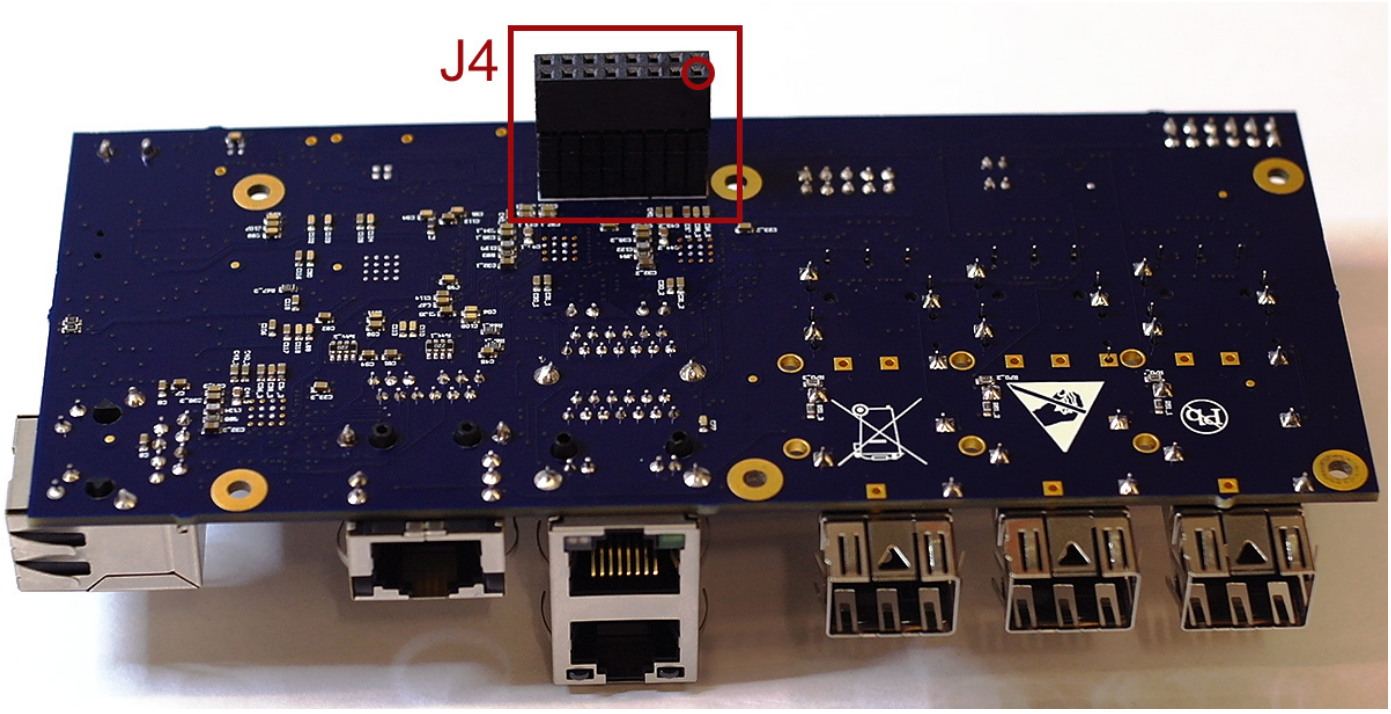


Table 5. CPU/RPi Connector (J4) Pinout

Function	Connector Pin (left row)	Connector Pin (right row)	Function
+5 V	2	1	Not used
+5 V	4	3	I²C Data
GND	6	5	I²C Clock
MDIO1 Data	8	7	MDIO1 Clock
Not used	10	9	GND
Reset (active low)	12	11	Interrupt (active low)
GND	14	13	Power_OK
MDIO2 Data	16	15	MDIO2 Clock

2.5 JTAG

JTAG connector (J6) is for factory usage only.

2.6 GPIO

GPIO connector (J7) pinout is presented in Table 6. GPIO signals can be controlled by writing into XRS7004 registers. Each GPIO pin can be configured as an input or as an output independent from the other GPIO pins. The GPIO pins can be used for example for powering LEDs, or for implementing different kinds of communication interfaces, for example I²C, SPI, or MDIO. The I/O voltage is 3.3 V.

The pins are not 5 V tolerant.

Table 6. GPIO Connector (J7) Pinout

Function	Connector Pin (left row)	Connector Pin (right row)	Function
+3.3 V	1	2	GND
GPIO0	3	4	GND
GPIO1	5	6	GND
GPIO2	7	8	GND
GPIO3	9	10	GND

2.7 PPS

The pinout is presented in Table 7. The PPS output provides a 20 µs long pulse once a second. The rising edge of the PPS pulse is when the seconds value of the internal time of the XRS7004 chip is incremented. The resolution of the pulse is 8 ns.

The PPS/EVENT input is connected to EVENT[0] input (pin 8) of the XRS chip. The XRS chip counts and timestamps the rising edges of the signal (It can handle signals from 0 Hz to 25 MHz). The I/O voltage of the signals is 3.3 V.

The input is not 5 V tolerant.

Table 7. PPS Connector (J8, J9) Pinout

Function	Connector, Pin	Connector, Pin	Function
GND	J8, 1	J8, 2	PPS/EVENT in
GND	J9, 1	J9, 2	PPS out

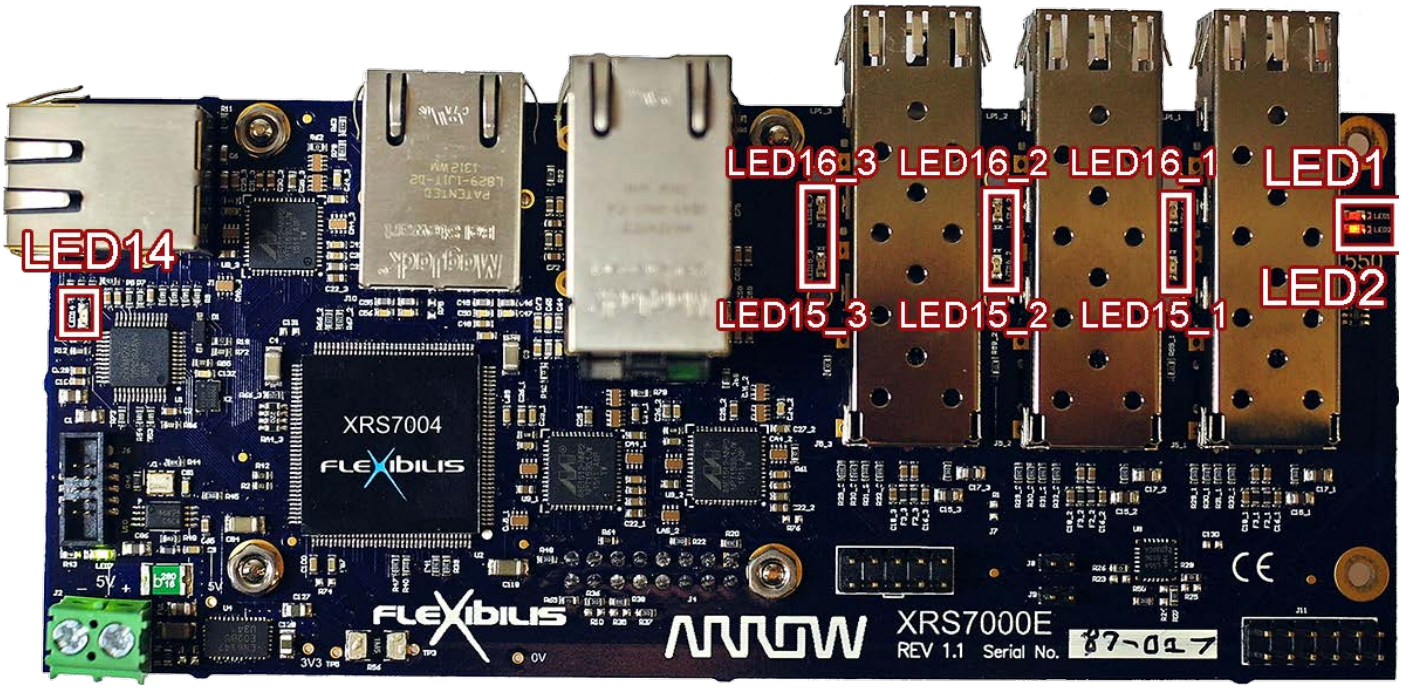
2.8 RFU

The RFU connector (J11) is reserved for future purposes. Currently it is only for Flexibilis internal use.

2.9 LEDs

The board has 17 LEDs. Combined to each RJ45 connector there are two LEDs, green and yellow. There are also green and yellow LEDs next to each SFP cage. In addition to these Ethernet interface LEDs there are three extra LEDs (marked as LED1, LED2 and LED14 in Figure 9) on the board.

Figure 9. LED locations



All the LEDs and their default usage are presented in Table 8.

Table 8. LEDs

LED	Marking	Controlled by	Color	Polarity
RJ45_0 left	-	PHY 0, LED_LINK	green	Active Low
RJ45_0 right	-	PHY 0, LED_SPEED	yellow	Active Low
Next to RJ45_0	LED14	PHY 0, LED_ACT	red	Active Low
RJ45_1 left	-	PHY 1, LED0	green	Active High
RJ45_1 right	-	XRS GPIO17	yellow	Active High
RJ45_2 left	-	PHY 2, LED0	green	Active High
RJ45_2 right	-	XRS GPIO18	yellow	Active High
RJ45_3 left	-	PHY 3, LED0	green	Active High
RJ45_3 right	-	XRS GPIO19	yellow	Active High
SFP1 green	LED16_1	PHY 1, LED1	green	Active High
SFP1 yellow	LED15_1	XRS GPIO12	yellow	Active High
SFP2 green	LED16_2	PHY 2, LED1	green	Active High
SFP2 yellow	LED15_2	XRS GPIO13	yellow	Active High
SFP3 green	LED16_3	PHY 3, LED1	green	Active High
SFP3 yellow	LED15_3	XRS GPIO14	yellow	Active High
User LED1	LED1	XRS GPIO15	green	Active High
User LED2	LED2	XRS GPIO16	red	Active High

3. EXAMPLE TEST SETUPS

This chapter presents a couple of test setups that can be used to test and evaluate the functionality of XRS7000 chip. Note that a CPU board and a software running on the CPU, controlling the XRS7000 Reference Board functionality, is needed. Reference software for XRS devices is described in another document, XRS_Reference_Software_User_guide.pdf.

Figure 10 presents a test setup for testing HSR functionality. A traffic generator/analyzer is used to transmit traffic to the network, and to check whether frames are received without errors from the network. The laptop can be used to configuring and changing the settings of the devices as well as checking for example values of the device internal counters.

During traffic tests any of the Ethernet links of the HSR ring can be disconnected and connected again. When only one link is disconnected at a time, it is not allowed to cause any frame loss, but reordering of a few frames may occur when links are reconnected.

Figure 10. Example HSR Test Setup

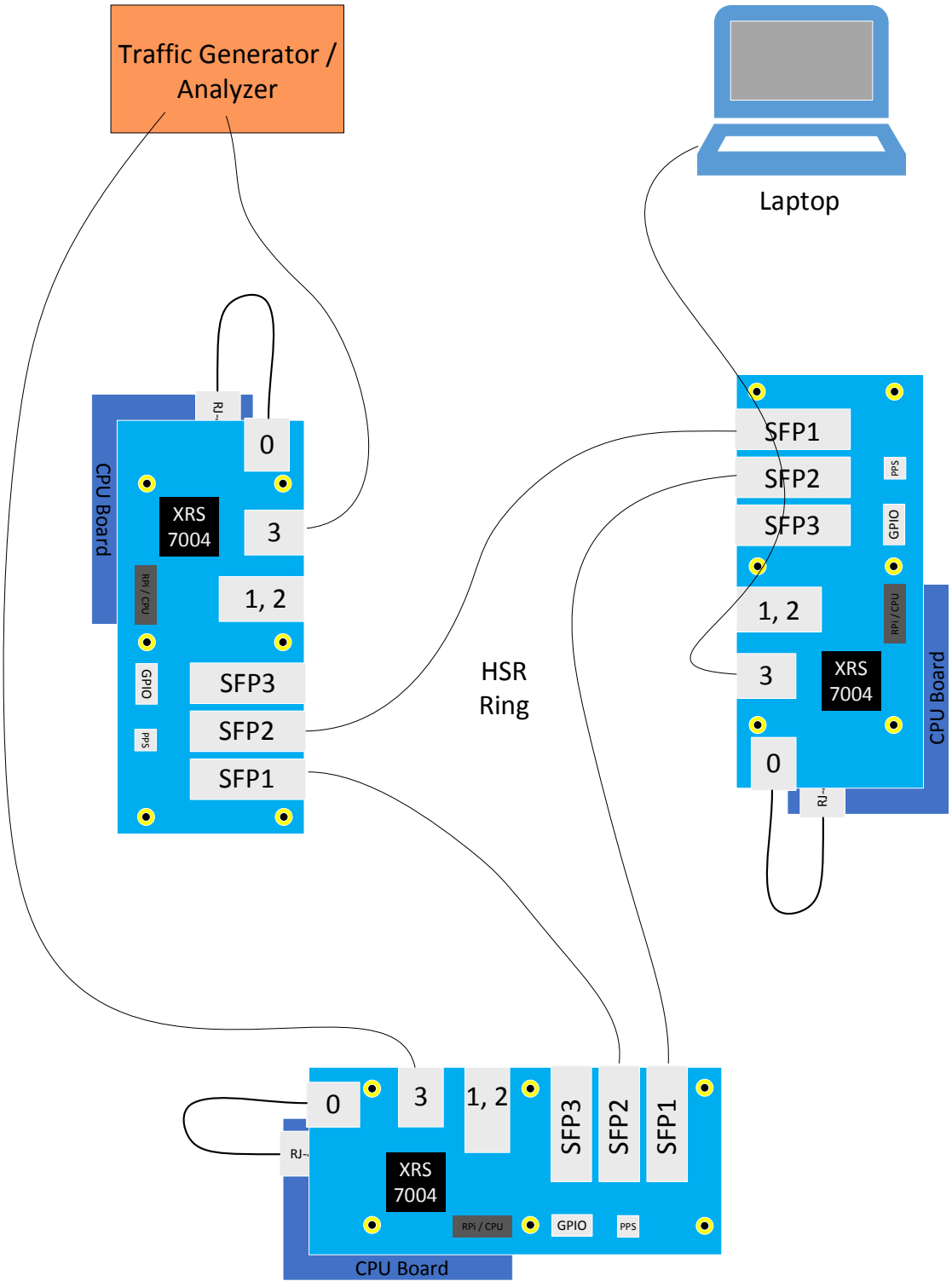


Figure 11 presents a test setup for testing PRP functionality. A traffic generator/analyzer is used to transmit traffic to the network, and to check whether frames are received without errors from the network. The laptop can be used to configuring and changing the settings of the devices as well as checking for example values of the device internal counters.

During traffic tests any of the PRP links of either one of the PRP LANs can be disconnected and connected again. This is not allowed to cause any frame loss, but reordering of a few frames may occur when links are reconnected. Also either one of the PRP LAN center switches can be powered off during tests.

Figure 11. Example PRP Test Setup

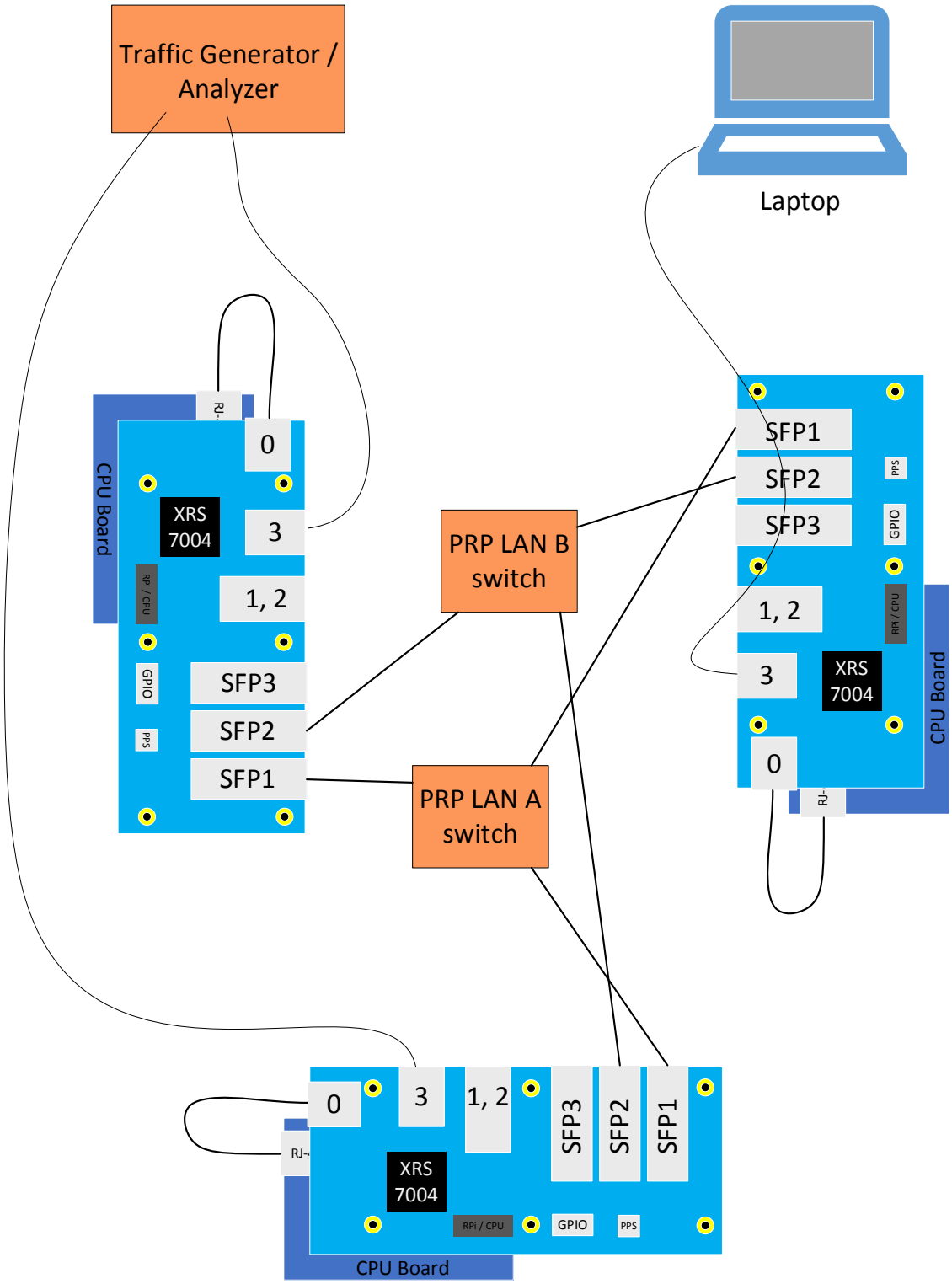
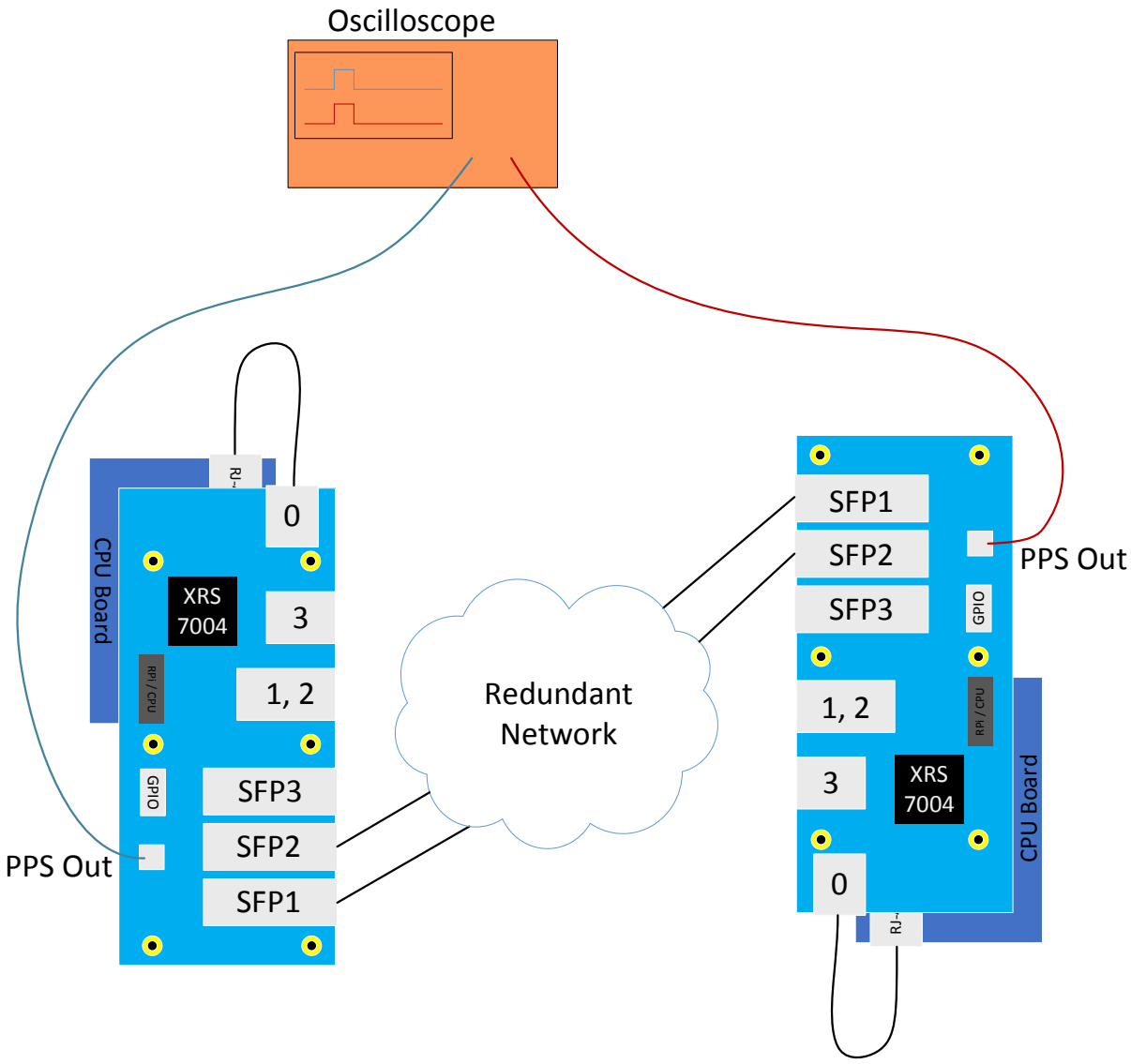


Figure 12 presents a test setup for testing IEEE 1588 Precision Time Protocol (PTP) functionality. Optionally a laptop can be used for configuring and changing the settings of the devices as well as checking for example master/slave statuses of the devices and the reported synchronization accuracy. It is also possible to add traffic generator/analyzer to this test setup, to generate extra traffic to the network like in Figure 10 and Figure 11. But this test can be run well also without a computer or traffic generator.

The redundant network can be either HSR or PRP. The IEEE 1588 Best Master Selection (BMS) protocol selects the other device to be a PTP Slave and the other device to be a PTP Master.

The XRS7000 Reference Boards have PPS output connectors that provide a PPS pulse of length 20 µs once a second. An oscilloscope or time interval counter can be used to compare how much difference in time the rising edges of the PPS pulses from different boards have. This is the time synchronization error between the boards..

Figure 12. Example IEEE 1588 PTP Test Setup



ARROW FLEXIBILIS Five Years Out

4. ORDERING INFORMATION

4.1 Ordering Numbers

Ordering numbers for Reference Boards are presented in Table 9.

Table 9. Part Ordering Numbers

Reference board	XRS7000 Package	Board Ordering Number
XRS7004 Reference Board	EQFP144	ARWSCBRD-XRS7004E

What is included:

- XRS7000 Reference Board

What is not included (have to be purchased separately):

- CPU board (For example Raspberry Pi 2 Model B)
- Memory card for the CPU board (if needed, Raspberry Pi needs a micro SD card)
- Power Supply (5 V, 3 A)
- Standoffs/spacers for the board(s) (M3 is too large diameter, M2.5 is OK. The distance between Raspberry and XRS boards should be 21.2 mm…23 mm.)
- Copper Ethernet cables (RJ45)
- Fiber optic Ethernet cables (SFP modules typically have LC connectors)
- SFP modules

4.2 Sales Offices

Arrow has more than 460 locations worldwide. An up to date list of Arrow sales offices and contact information is available at Arrow web page:

http://arrow.com/office_locations/

Arrow International telephone number (Europe, South America, Africa, Asia and Oceania): +800-8000-1010

Arrow telephone number (Canada, United States): 1-855-326-4757